Day 1 September 13 Wednesday

Venue	Room 504a	Room 504b	Room 504c
13:30-16:50	Tutorial I Automotive Test	Tutorial II 3D-IC Test	Tutorial III Yield Learning

Day 2 September 14 Thursday

Venue	Room 504abc		
	Opening Remarks		
09:00-10:50	Keynote Session I K1: Hardware Security - Verification, Test, and Defense Mechanisms - Tim Cheng K2: Convergence of Electronic and Semiconductor Systems, and Its Impact on Testing Technology - I-Shih Tseng		
10:50-11:10	Coffee Break		
11:10-12:30	Plenary Panel Heterogeneous Integration – Design and Test Challenges		
12:30-13:50	Lunch Break		
Venue	Room 504a	Room 504b	Room 504c
13:50-15:05	Session A1: Corporate Session I (Invited)	Session B1: Analog / Mixed-Signal Test	Session C1: Cell-Aware Testing
15:20-17:00	Session A2: Corporate Session II (Invited)	Session B2: Detection, Diagnosis, and Debug	Session C2: Test for IoTs and Automotives
18:30-21:00	Banquet		

Day 3 September 15 Friday

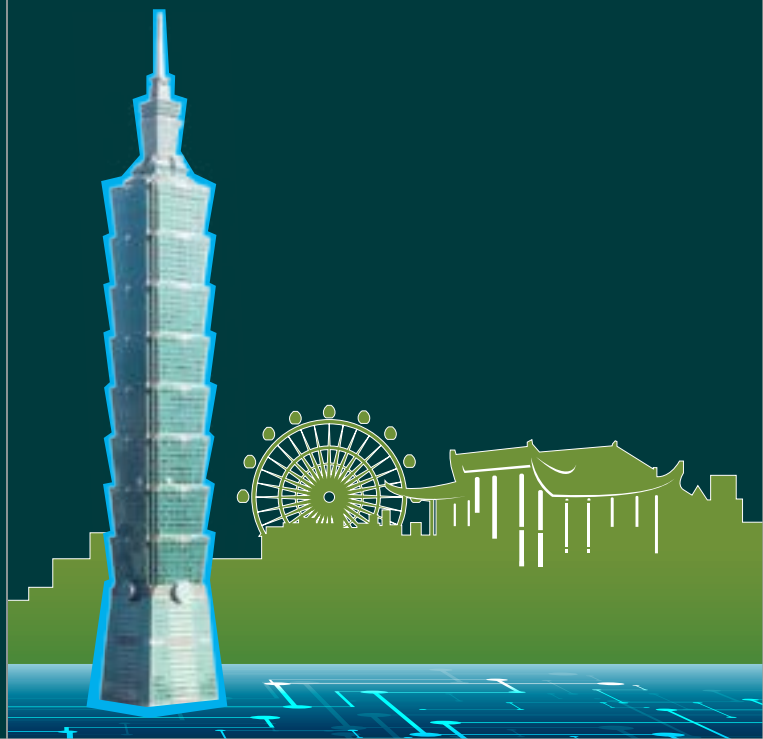
Venue	Room 504abc		
09:00-10:30	Keynote Session II K3: Seven Major Trends that are Changing how we Test Ics - Phil Nigh K4: Test Emerging Memories - Rob Aitken		
10:30-10:50	Coffee Break		
Venue	Room 504a	Room 504b	Room 504c
11:00-12:15	Session A3: EDA Session (Invited)	Session B3: Test for InFO and SoC	Session C3: Memory Testing
12:15-13:50	Lunch Break		
Venue	Room 504a	Room 504b	Room 504c
13:50-15:05	Session A4: Fabless and IDM Session (Invited)	Session B4: On-Chip Test Infrastructure	Session C4: Advanced Test Practices
15:20-17:00	Session A5: OSAT Session (Invited)	Session B5: Verification and Fault Tolerant	Session C5: Embedded Tutorials (Invited)

Printed on September 1, 2017

ITC-Asia 2017
International Test Conference in Asia

September 13-15, 2017
Taipei, Taiwan

PROGRAM BOOK



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FOREWORD

Welcome to the first International Test Conference in Asia (ITC-Asia 2017)!

International Test Conference organized by IEEE has long been the world's most premier conference dedicated to the electronic testing and validation. In order to lead our semiconductor community forward with increasing globalization and worldwide cooperation, IEEE takes an initiation to launch this new conference, namely "International Test Conference in Asia," (abbreviated as ITC-Asia), to be held for the first time in Taipei, Taiwan, on Sept. 13-15, 2017.

This conference addresses the grand challenge of the quality insurance of electronic systems incorporating more and more sophisticated manufacturing processes and system integration technologies in various emerging applications including Internet of Things, cloud computing, automotive electronics, etc. Main themes to be explored include test development and design validation/verification for super-complex multi-die 3D-ICs, hardware security for IoT devices, zero-defect test requirement and reliability enhancement for automotive electronics.

ITC-Asia 2017 is designed to be co-located with SEMICON Taiwan 2017 (which attracts more than 40,000 attendees in each of recent three years), with an attempt to stimulate a closer relationship between the research community and the global industry. In light of this objective, participation from the industry is a vital part. In addition to the presentations of 28 research papers, we have further enriched the contents of this conference with the arrangements of 3 half-day tutorials, 4 keynote speeches, 1 panel, 3 embedded tutorials, and more than 10 invited talks. An exhibition attracting more than 20 companies to demonstrate their most recent techniques and products are also arranged. We sincerely hope that ITC-Asia will become an important annual gathering in Asia for people and companies around the globe to share the state-of-the-art test and validation technologies for emerging electronic systems.

On behalf of the steering committee and organizing committee, we cordially thank you again for your participation to make this first ITC-Asia event successful.

Prof. Cheng-Wen Wu
(Steering Comm. Chair)

National Tsing Hua University, Taiwan
cww@ee.nthu.edu.tw

Prof. Kuen-Jong Lee
(General Co-Chair)

National Cheng Kung University, Taiwan
kjlee@mail.ncku.edu.tw

Prof. Li-C. Wang
(General Co-Chair)

Univ. of California,Santa Barbara, USA
liwang@ece.ucsb.edu.tw

Prof. Shi-Yu Huang
(Program Chair)

National Tsing Hua University, Taiwan
syhuang@ee.nthu.edu.tw

Foreword

SEMICON® TAIWAN

About SEMICON Taiwan
國際半導體展

SEMICON Taiwan is the premier event in Taiwan for microelectronics manufacturing. Connect with the companies, people, products and information shaping the future of design and manufacturing for semiconductors, nanoelectronics, MEMS, Photo-voltaics and related advanced electronics.

The Largest Microelectronics Event in Taiwan

- Taiwan Claimed the Largest Market for New Semiconductor Equipment for the Fifth Year in a Row
- Over 700 Exhibitors from the Globe Covering more than 1,700 Booths
- Expected to Attract Over 43,000 Visitors and 3,300 Program Participants in 2017
- 45% of the visitors are above management level and 52% with purchasing power

Website: http://www.semicontaiwan.org/en/

ITC-Asia 2017 Banquet

Date:
Thursday, September 14th, 2017

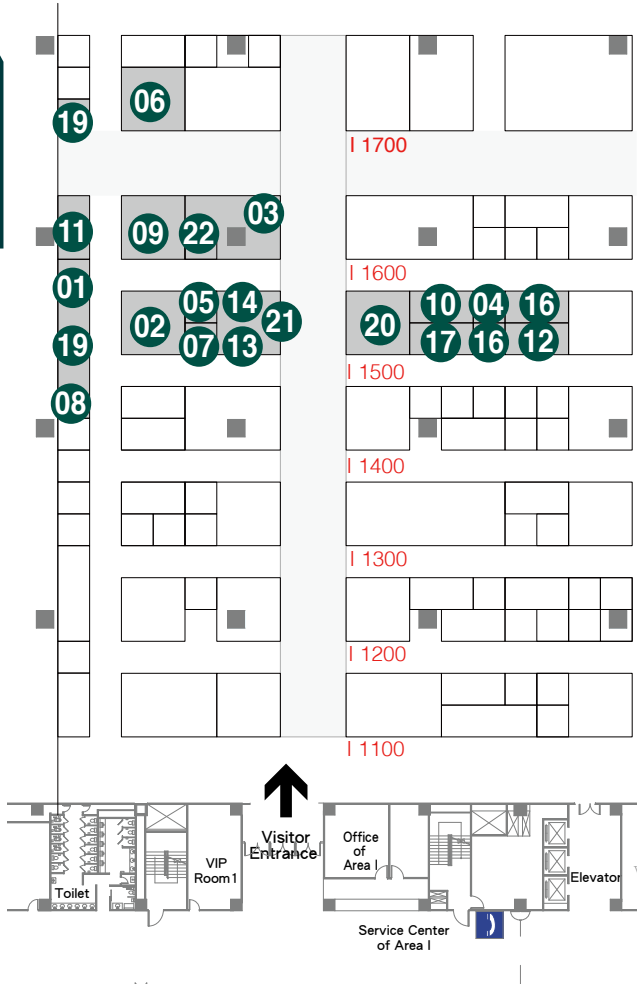
Time:
18:30-21:00

Venue:
Supernova Ballroom, Courtyard Taipei
六福萬怡酒店 超新星大宴會廳

Address:
7F, No 359 Section 7 Zhongxiao East Road, Nangang District, Taipei City, Taiwan
台北市南港區忠孝東路七段359號7樓

Fee:
Ticket Required. We invite All Pass and Full Conference attendees to join the banquet.
*Student registration excluded

ITC-ASIA EXHIBITION



Venue:

I area, 1F, Taipei Taipei Nangang Exhibition Center, Hall 1

Show Hours:

10:00-17:00, September 13 to September 14

10:00-16:00, September 15

01	AEHR	Aehr Test SystemsFremont, CA, United States, **Booth 2014,** http://www.aehr.com
02	Aemulus	Aemulus Corporation Sdn Bhd. Corporation, Bayan Lepas, Penang, Malaysia **Booth 1508,** http://www.aemulus.com
03	Chroma	Chroma ATE Inc. Taoyuan City, Taiwan **Booth 1616,** http://www.chromaate.com
04	CTS Cloud Testing Service	Cloud Testing Service, Inc.Chiyoda-ku, Tokyo, Japan **Booth 1627,** https://www.cts-advantest.com
05	CRYSTAL KING	Crystal King Co., Ltd.Taipei City, Taiwan **Booth 1613,** http://www.crystalking.com.tw
06	DJT	D J Tech Chip Test Co. Kaohsiung City, Taiwan **Booth 1708,** http://www.djt.com.tw
07	EDA Industries	EDA Industries S.p.a. Cittaducale (RI), Italy **Booth 1512,** https://www.eda-industries.net
08	GLTTEK	GLTTEK CO.,LTD. Hsinchu City, Taiwan **Booth 2010,** http://glttek.com
09	ISC	ISC Co., Ltd. Incheon, Korea (South) **Booth 1608,** http://isc21.kr
10	JEM	JAPAN ELECTRONIC MATERIALS CORPORATION Amagasaki-shi, Hyogo, Japan **Booth 1623,** http://www.jem-net.co.jp
11	KZT	Kaizhitong Micro-Electronic Technology Co., Ltd. Shenzhen, China **Booth 2015,** http://www.icsocket.net
12	OKins	OKins Electronics, Uiwang-si, Gyeonggi-do, Korea (South) **Booth 1528,** http://www.okins.co.kr
13	PDF SOLUTIONS	PDF Solutions, Inc. San Jose, CA, United States **Booth 1514,** https://www.pdf.com
14	recynergy 瑞勝捷科技	recynergy Technology., Inc Hsinchu City, Taiwan **Booth 1514-1,** http://www.recynergy.com
15	SEIKEN	Seiken Micro Technology Co., Ltd. Taoyuan City, Taiwan **Booth 1629,** http://web.seiken.com.tw
16	SER	S.E.R. Corporation, Shinagawa-ku, Tokyo, Japan **Booth 1526,** http://www.ser.co.jp
17	SYNOPSYS	Synopsys Taiwan Ltd. Taipei City, Taiwan **Booth 1522,** https://www.synopsys.com
18	Tesec	Tesec Corporation, Tokyo, Japan **Booth 2012,** http://en.tesec.co.jp
19	testinsight	Test Insight, Ramat-Gan, Israel **Booth 2017,** http://www.testinsight.com
20	TSE	TSE Co., Ltd. Cheonan-si, Chungnam, Korea (South) **Booth 1518,** http://www.tse21.com
21	TSSI	Test Systems Strategies, Inc. Beaverton, OR, United States **Booth 1514-2,** https://www.tessi.com
22	Tulip	Tulip Co., Ltd. Hiroshima, Japan **Booth 1612,** http://en.tulip-japan.co.jp

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NXP

Shiyi Xu
Shanghai University

Qiang Xu
The Chinese University of Hong Kong

OVERALL AGENDA

Day 1 September 13 (Wednesday)

Venue	Room 504a	Room 504b	Room 504c
13:30-16:50	Tutorial I Automotive Test	Tutorial II 3D-IC Test	Tutorial III Yield Learning
	Coffee Break		
	Tutorial I Automotive Test	Tutorial II 3D-IC Test	Tutorial III Yield Learning

Day 2 September 14 (Thursday)

Venue	Room 504abc		
09:00-10:50	Opening Remarks Keynote Session I K1: Hardware Security - Verification, Test, and Defense Mechanisms - Tim Cheng K2: Convergence of Electronic and Semiconductor Systems, and Its Impact on Testing Technology - I-Shih Tseng		
10:50-11:10	Coffee Break		
Venue	Room 504abc		
11:10-12:30	Plenary Panel Heterogeneous Integration – Design and Test Challenges		
12:30-13:50	Lunch Break		
Venue	Room 504a	Room 504b	Room 504c
13:50-15:05	Session A1: Corporate Session I (Invited)	Session B1: Analog / Mixed-Signal Test	Session C1: Cell-Aware Testing
14:45-15:00	Coffee Break		
Venue	Room 504a	Room 504b	Room 504c
15:20-17:00	Session A2: Corporate Session II (Invited)	Session B2: Detection, Diagnosis, and Debug	Session C2: Test for IoTs and Automotives
Venue	Supernova Ballroom, Courtyard Taipei		
18:30-21:00	Banquet		

Day 3 September 15 (Friday)

Venue	Room 504abc		
09:00-10:30	Keynote Session II K3: Seven Major Trends that are Changing how we Test Ics - Phil Nigh K4: Test Emerging Memories - Rob Aitken		
10:30-10:50	Coffee Break		
Venue	Room 504a	Room 504b	Room 504c
11:00-12:15	Session A3: EDA Session (Invited)	Session B3: Test for InFO and SoC	Session C3: Memory Testing
12:15-13:50	Lunch Break		
Venue	Room 504a	Room 504b	Room 504c
13:50-15:05	Session A4: Fabless and IDM Session (Invited)	Session B4: On-Chip Test Infrastructure	Session C4: Advanced Test Practices
15:05-15:20	Coffee Break		
Venue	Room 504a	Room 504b	Room 504c
15:20-17:00	Session A5: OSAT Session (Invited)	Session B5: Verification and Fault Tolerant	Session C5: Embedded Tutorials (Invited)

- Half-Day Tutorials
- Corporate Session
- Embedded Tutorial
- Technical Session
- Keynote Session
- Industrial Session
- Plenary Panel
- Event

HALF-DAY TUTORIALS

Date: September 13
Time: 13:30-16:50
Session: Tutorial I

Location: Room 504a
Session Chair: Shi-Yu Huang

Automotive Test Strategies

Yervant Zorian
Synopsys

Given today's fast growing automotive semiconductor industry, this tutorial will discuss the implications of automotive test, reliability and functional safety requirements on all aspects of the SOC lifecycle: design, silicon bring-up, volume production, and particularly in-system functional safety. Today's automotive safety critical chips need multiple in-system self-test modes, such as power-on self-test and repair, periodic in-field self-test, advanced error correction, etc. This tutorial will cover these specific in-system modes and the benefits of selecting ISO 26262 certified solutions to ensure standardized functional safety requirements, while accelerating time to market for automotive SOCs.

Date: September 13
Time: 13:30-16:50
Session: Tutorial II

Location: Room 504b
Session Chair: Jin-Fu Li

Testing of 2.5D- and 3D-Stacked Integrated Circuits

Erik Jan Marinissen
IMEC

After a long period of technology hype, finally real 3D-stacked IC products containing through-silicon vias and micro-bumps (and also their interposer-based 2.5D-SIC variant) are hitting the market. Testing of 2.5D- and 3D-SICs is fraught with new test and design-for-test challenges, for which solutions are only emerging. The test challenges are the following. (1) Test flows: what to test for when? (2) Test content: do these stacked ICs bring new defects and faults and how do we test for those? (3) Test access: how do we pump in/out the test stimuli/responses into the dies and die stacks? In this tutorial, we present the fundamentals of 3D fabrication processes, defects, and fault modeling. We discuss test flows and present test-flow cost modeling and optimization. The tutorial covers the most promising solutions for pre-bond and post-bond (stack) testing, including advances in 3D probe technology, advanced 3D-DfT architectures and optimization, and the ongoing IEEE P1838 standardization effort for test access.

September 13, Day 1

Date: September 13
Time: 13:30-16:50
Session: Tutorial III

Location: Room 504c
Session Chair: Chien-Mo Li

Industrial Advancements in Diagnosis Driven Yield Analysis

Yu Huang, Wu Yang, and Wu-Tung Cheng
Mentor, A Siemens Business

Delivering a stable high yield product on time is the ultimate goal for the semiconductor industry. With the increasing complexity of design and processes, too often, the yield is lower than expected or takes longer to ramp to the target level. Scan diagnosis driven yield analysis (DDYA) can expedite the debug and analysis process reducing the time-to-market and minimizing the related cost. Identifying systematic defects, understanding the root causes of the systematic defect and selecting the right die and suspect candidate for physical failure analysis (PFA) are important components for yield analysis. The recent technology advances in scan chain diagnosis, layout-aware and cell-aware diagnosis can provide fast, high resolution and accurate volume diagnosis data used in the aforementioned steps.

Based on volume diagnosis results, different analysis techniques are developed to help identify the systematic defects. These methodologies include the systematic suspect location analysis, wafer zonal analysis, design-for-manufacturing (DFM) correlation analysis, root-cause deconvolution (RCD) and some others. RCD is a statistical analysis method utilizing Bayesian model. It calculates the defect weight probability with the design information and diagnosis results. It provides a direct or visual defect distribution pareto based on maximum likelihood and further helps drill down to the correspondent die and suspect for each root cause, which can be used for PFA. In this DDYA solution, the PFAs on the selected die and suspect candidates are to validate the findings on the systematic root causes. Hence it greatly reduces the efforts, costs and time for yield analysis. The tutorial will review the recent industrial advancements in the above three areas and each topic will be covered for about 50 minutes.

Date: September 14
Time: 09:00-10:50
Session: Keynote Session I

Location: Room 504abc
Session Chair: Shi-Yu Huang

Keynote - 1
Hardware Security - Verification, Test, and Defense Mechanisms

Tim Cheng
Hong Kong U. of Science and Technology

In this talk I will illustrate several types of Hardware Trojans and security threats they create, as well as opportunities of Trojan insertion in all steps of the design, fabrication, and testing processes. I will then discuss their defense mechanisms, verification techniques for Trojan detection and prevention, and test-specific need and challenges for hardware security.

About the speaker

Tim Cheng received his Ph.D. in EECS from the University of California, Berkeley in 1988. He has been serving as Dean of Engineering and Chair Professor of ECE and CSE at Hong Kong University of Science and Technology (HKUST) since May 2016. He worked at Bell Laboratories from 1988 to 1993 and joined the faculty at Univ. of California, Santa Barbara in 1993 where he was the founding director of UCSB's Computer Engineering Program (1999-2002), Chair of the ECE Department (2005-2008) and Associate Vice Chancellor for Research (2013-2016). His current research interests include hardware verification and security, design automation for photonics IC and flexible hybrid circuits, memristive memories, mobile embedded systems, and mobile computer vision. He has published more than 400 technical papers, co-authored five books, adviced 40+ PhD theses, and holds 12 U.S. Patents in these areas. Cheng, an IEEE fellow, received 10+ Best Paper Awards from various IEEE and ACM conferences and journals. He has also received UCSB College of Engineering Outstanding Teaching Faculty Award. He served as Editor-in-Chief of IEEE Design and Test of Computers and was a board member of IEEE Council of Electronic Design Automation's Board of Governors and IEEE Computer Society's Publication Board.

KEYNOTE SESSION I

Date: September 14
Time: 09:00-10:50
Session: Keynote Session I

Location: Room 504abc
Session Chair: Kuen-Jong Lee

Keynote - 2
Convergence of Electronic and Semiconductor Systems, and Its Impact on Testing Technology

I-Shih Tseng
Chroma ATE Inc.

As electronic systems are increasingly dominated by system ICs, convergence of electronic system test and semiconductor test is now essential. Environmental variances and stresses often plays vital role in yield or reliability of both system IC and electronic systems. Testing system variables on ICs can significantly enhance reliability of final systems, but also becomes one of major testing challenges for IC vendors. Electronic system also comprises multiple physical interfaces, like optical light, mechanical vibration, temperature, or even chemical contents. Such integration is now migrated upstream into semiconductor process or substrate process. Semiconductor test is no longer just digital or analog test. Integration of wide variety of measurement instruments also pose tremendous challenges not only to test equipment vendors, also to manufacturing operators. The effort and challenges in those two areas will be discussed, primarily from equipment vendor point of view.

About the speaker

Dr. I-Shih Tseng is the President of Chroma ATE Inc. He joined Chroma in 1998 and involved in the development of semiconductor test equipment. Other positions I-shih served at Chroma including Deputy Chief Engineer, Research Vice President, Semiconductor Test Equipment Business Unit President, Chief Technology Officer, and President of Integrated System Solution BU. Particularly in semiconductor test solution, Chroma provides VLSI test system, SoC/analog test system, system/final level tri-temp test handler, and PXI/PXIe IC test platform. He is also the Chairman of ADIVIC Corporation. I-Shih received his Ph.D. in mechanical engineering from The Pennsylvania State University, Penn., and B.S. from National Taiwan University. His technical expertise includes semiconductor testing system, system automation, and mechanical engineering.

September 14, Day 2

Date: September 14
Time: 11:10-12:30
Session: Plenary Panel

Location: Room 504abc
Organizer and Moderator: Cheng-Wen Wu

Heterogeneous Integration – Design and Test Challenges

Panelists:

- ***Jason Hsu, MediaTek***
- ***Edward Lee, RealTek***
- ***Yervant Zorian, Synopsys***
- ***Roger Hwang, ASE***
- ***Erik Jan Marinissen, IMEC***
- ***Shih-Lien Lu, TSMC***

It is of utmost importance to smart handheld devices and many advanced IOT applications that we should continue to improve the power efficiency and reduce the cost of a system, and for such system to obtain both high data bandwidth and high system performance in a small form factor. As Moore's Law is slowing down, advanced heterogeneous 3D and 2.5D integration is gradually taking over the key role for that purpose. However, there are design and test challenges that we need to deal with. In this panel, we invite expert panelists to address and discuss challenges, potential solutions, and cases from different angles of view. The panel will also give comparisons among SOC, SiP, MCM, PoP, InFO, 3D-IC, etc. The audience are welcome to interact with the panelists by giving comments and asking questions.

Date: September 14
Time: 13:50-15:05
Session A1: Corporate Session I (Invited)

Location: Room 504a
Session Chair: Seiji Kajihara

(A1-1)
The Trend of Testing on IoT Ics
George Chang
Chroma ATE Inc.

(A1-2)
Economic Trade-off in Probe Card Solutions
Daniel Chen
JEM Taiwan

(A1-3)
Improved Test Quality and Efficiency via Better Link of Design and Test
Meir Gellis
Test Insight Ltd.

Date: September 14
Time: 13:50-15:05
Session B1: Analog and Mixed-Signal Test

Location: Room 504b
Session Chair: Soon-Jyh Chang

(B1-1)
Low-Distortion Signal Generation for Analog/Mixed-Signal Circuit Testing with Digital ATE
*Masayuki Kawabata, Koji Asami, Shohei Shibuya, *Tomonori Yanagida, and Haruo Kobayashi*
Advantest Corporation and Gunma University

(B1-2)
A Quick Jitter Tolerance Estimation Technique for Bang-bang CDRs
**Yen-Long Lee and Soon-Jyh Chang*
National Cheng Kung University

(B1-3)
Evaluation of Loop Transfer Function Based Dynamic Testing of LDO
Mehmet Ince, Sule Ozev, Ender Yilmaz, Jae Woong Jeong, and Leroy Winemberg
Arizona State University and NXP

Date: September 14
Time: 13:50-15:05
Session C1: Cell-Aware Test

Location: Room 504c
Session Chair: Martin Keim

(C1-1) (Invited)
The Role of Test in Advanced System Design – Challenges & Opportunities
**Yin Wang*
Cadence Design Systems

(C1-2)
Test Generation for Open and Delay Faults in CMOS Cells
**Cheng-Hung Wu, Kuen-Jong Lee, and Sudhakar M. Reddy*
National Cheng Kung University and University of IOWA

(C1-3)
Cell-Aware Test Time Reduction by Using Switch-Level ATPG
**Po-Yao Chuang, Cheng-Wen Wu, and Harry H. Chen*
National Tsing Hua University and MediaTek Inc.

Date: September 14
Time: 15:20-17:00
Session A2: Corporate Session II (Invited)

Location: Room 504a
Session Chair: Mango (Chia-Tso) Chao

(A2-1)
Cadence Modus Test Solution
Yin Wang
Cadence Design Systems

(A2-2)
Silicon Test Solutions for Giga-gate SOC Designs and Automotive Ics
Wu Yang
Mentor, A Siemens Business

(A2-3)
Improved ON-resistance Measurement at Wafer Probe using "DARUMA" stage of ACCRETECH UF2000
Yuichi Kakizaki
TESEC Corporation

(A2-4)
Testing Modern Devices with Modern Tools
Hau Lam
Test Systems Strategies, Inc.

Date: September 14
Time: 15:20-17:00
Session B2: Detection, Diagnosis, and Debug

Location: Room 504b
Session Chair: Tong-Yu Hsieh

(B2-1)
GPU Accelerated Fault Dictionary Generation for the TRAX Fault Model
**Matthew Beckler and Shawn Blanton*
Carnegie Mellon University

(B2-2)
Physical-aware Diagnosis of Multiple Interconnect Defects
Jing-Yu Chen, Po-Hao Chen, Chi-Lin Lee,
**Po-Wei Chen, and Chien-Mo Li*
National Taiwan University

(B2-3)
A Run-Pause-Resume Silicon Debug Technique for Clock Domain
**Shuo-Lian Hong and Kuen-Jong Lee,*
National Cheng Kung University

(B2-4)
A Hybrid Concurrent Error Detection Scheme for Simultaneous Improvement on Probability of Detection and Diagnosability
**Chih-Hao Wang and Tong-Yu Hsieh*
National Sun Yat-Sen University

Date: September 14
Time: 15:20-17:00
Session C2: Test for IoT and Automotives

Location: Room 504c
Session Chair: Charles H.-P. Wen

(C2-1)
A Dependable AMR Sensor System for Automotive Applications
*Andreina Zambrano and *Hans G. Kerkhoff*
University of Twente

(C2-2)
An Automotive MP-SoC Featuring an Advanced Embedded Instrument Infrastructure for High Dependability
Hans G. Kerkhoff, Ghazanfar Ali, Hassan Ebrahimi, and Ahmed Ibrahim
University of Twente

(C2-3)
Symbiotic System Models for Efficient IOT System Design and Test
**Cheng-Wen Wu, Bing-Yang Lin, Hsin-Wei Hung, Shu-Mei Tseng, and Chi Chen*
National Tsing Hua University

(C2-4)
A Lightweight X-Masking Scheme for IoT-Designs
**Daniel Tille, Benedikt Gottinger, and Ulrike Pfannkuchen*
Infineon Technologies AG

Date: September 15
Time: 09:00-10:50
Session: Keynote Session II

Location: Room 504abc
Session Chair: Li-C. Wang

Keynote - 3
Seven Major Trends that are Changing how we Test ICs

Phil Nigh
GLOBALFOUNDRIES

Products such as mobile processors, Automotive ICs, 5G ICs and the slowdown of technology scaling are changing how we perform development & production testing. In this talk, I'll summarize the 7 trends driving change – and describe how the test industry must change given these emerging requirements.

- Automotive ICs – achieving extreme Quality & Reliability & Cost requirements while enabling online, continuous testing in the field. (including advanced fault models, test coverage metrics and analytical methods)
- Multichip Products (such as 2.5D and MCMs) – industry-wide Test collaboration is required to achieve the vision of the Heterogeneous Integration Industry Roadmap (integrating KGD/bare die from multiple suppliers)
- E2E Data Analytics Collaboration – enabling Adaptive Testing (for cost & quality) and cross-company analytics for Test optimization (including OSAT data feedforward & analytic methods)
- 5G/mmWave/RF/Silicon Photonics – we need robust, flexible production test capability instead of point solutions
- Technology scaling is driving decreased performance margins – requiring different test approaches and design resilience for long-term field reliability
- Rapid time-to-volume – IC testing now has a major role in driving fab & design learning (e.g., yield) – production testing methods need to significantly improve to enable faster yield ramping
- Component System-level Testing (SLT) – should we be driving to avoid SLT … or embrace it? How does ATE production testing change if we accept SLT is required?

About the Speaker

Dr. Phil Nigh is a Distinguished Member of Technical Staff and has been a Test Engineer for over 34 years at IBM and GLOBALFOUNDRIES and is responsible for defining & driving Test Strategy including test methods, design-for-test, diagnostic methods and Adaptive Testing. Phil received his PhD from Carnegie Mellon University in 1990. Phil received the Best Paper award at the International Test Conference in 1999 and has done a number of keynote addresses at conferences and workshops and has over 40 world-wide patents. He has organized the "Industry Test Challenges" workshop for over 15 years.

KEYNOTE SESSION II

Date: September 15
Time: 09:00-10:50
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Location: Room 504abc
Session Chair: Harry Chen

Keynote - 4
Test Emerging Memories

Rob Aitken
ARM

As device scaling slows down, memories are among the hardest hit circuits. Bit cell dimensions push the limits of design rules, and dense structures make achieving high yields difficult, even with the regularity of memory structures. The workhorse memories of the last twenty years, SRAM, DRAM and NAND flash are all facing significant challenges going forward. While the dominant technologies have struggled, some radically new memory technologies have been proposed to take their place. This talk looks at what these technologies are and where they fit within the memory hierarchy, but also looks at their test implications: What failure modes are likely? How can a resistive crosspoint be tested? What redundancy and repair methods make sense and what yield issues can they cover? Answering these questions is key to commercial success for emerging memories, but the answers are different enough that some of our intuition about memory test will need replacing in order to reflect a new reality.

About the speaker

Rob Aitken is an ARM Fellow responsible for technology direction at ARM Research. He works on low power design, technology roadmapping, and next generation memories. He has worked on 15+ Moore's law nodes and has published over 80 technical papers, on a wide range of topics. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He holds a Ph.D. from McGill University in Canada. Dr. Aitken is an IEEE Fellow, and serves on a number of conference and workshop committees.

September 15, Day 3

Date: September 15
Time: 11:00-12:15
Session A3: EDA Session (Invited)

Location: Room 504a
Session Chair: Jiun-Lang Huang

(A3-1)
The Emerging Applications of Machine Learning in Testing
Yu Huang
Mentor, A Siemens Business

(A3-2)
Integrated Electrical and Thermal Analysis flow for Integrated Fan-Out(InFO) Wafer Level Package
Charlie Shih
Cadence Design Systems

(A3-3)
Moving Test to RTL for High Testability, Functional Safety and Reliability
Dmitry Melnik
Synopsys

Date: September 15
Time: 11:00-12:15
Session B3: Test for InFO and SoC

Location: Room 504b
Session Chair: Hans Tsai

(B3-1)
Fan-Out Wafer Level Chip Scale Package Testing
**Hao Chen, Hung-Chih Lin, and Min-Jer Wang*
Taiwan Semiconductor Manufacturing Company

(B3-2)
Testing-for-Manufacturing (TFM) for Ultra-thin IPD on InFO
**Tang-Jung Chiu*
Taiwan Semiconductor Manufacturing Company

(B3-3) (Invited)
Test Strategy for Storage SoCs
*Abhishek Bhattacharya and *Ramesh Tekumalla*
Broadcom

September 15, Day 3

Date: September 15
Time: 11:00-12:15
Session C3: Memory Test

Location: Room 504c
Session Chair: Shyue-Kung Lu

(C3-1)
Adaptive Block-Based Refresh Techniques for Mitigation of Data Retention Faults and Reduction of Refresh Power
**Shyue-Kung Lu*
National Taiwan University of Science and Technology

(C3-2)
Software-Hardware-Cooperated Built-In Self-Test Scheme for Channel-Based DRAMs
**Tsung-Fu Hsien, Jin-Fu Li, Kuan-Te Wu, Jenn-Shiang Lai, Chih-Yen Lo, Ding-Ming Kwai, and Yung-Fa Chou*
National Central University and ITRI

(C3-3)
Adapting an Industrial Memory BIST solution for testing CAMs
Jais Abraham, Uttam Garg, Glenn Colon-Bonet, Ramesh Sharma, Chennian Di, Benoit Nadeau-Dostie, Etienne Racine, and Martin Keim
Guest Speaker: Kaitlyn Chen
Intel and Mentor, A Siemens Business

Date: September 15
Time: 13:50-15:05
Session A4: Fabless and IDM Session (Invited)

Location: Room 504a
Session Chair: Harry Chen

(A4-1)
DFT Challenges and Solutions for Automotive ICs
Ying-Yen Chen
RealTek Semiconductor Corp.

(A4-2)
Multi-Pronged Strategy to Reduce Scan Test Cost at Advanced Process Nodes
Jianguo Ren
MediaTek Inc.

(A4-3)
What Do We Do to Make System Reliable?
Xinli Gu
Huawei Technologies

Date: September 15
Time: 13:50-15:05
Session B4: On-Chip Test Infrastructure

Location: Room 504b
Session Chair: Hans Kerkhoff

(B4-1)
Reconfigurable Access to On-Chip Infrastructure
*Michael Kochte, *Rafal Baranowski, and Hans-Joachim Wunderlich*
University of Stuttgart

(B4-2)
On the Effects of Real Time and Contiguous Measurement with a Digital Temperature and Voltage sensor
**Yousuke Miyake, Yasuo Sato, and Seiji Kajihara*
Kyushu Institute of Technology

(B4-3)
Enhancing Security of Logic Encryption Using Embedded Key Generation Unit
**Rajit Karmakar, Santanu Chattopadhyay, and Rohit Kapur*
Indian Institute of Technology Kharagpur and Synopsys

Date: September 15
Time: 13:50-15:05
Session C4: Advanced Test Practices

Location: Room 504c
Session Chair: Ramesh Tekumalla

(C4-1)
A Mathematical Model to Assess the Influence of Parallelism in a Semiconductor Back-End Test Floor
Davide Appello, Mariapina Laurino, and Marco Pranzo
STMicroelectronics and Università di Siena

(C4-2)
A Fully Automatic Test System for Characterizing Large-Array Fine-Pitch Micro-Bump Probe Cards
Erik Jan Marinissen, Ferenc Fodor, Bart De Wachter, Joerg Kiesewetter, Eric Hill, and Ken Smith
IMEC and Cascade Microtech, Inc.

(C4-3)
Test Item Priority Estimation for High Parallel Test Efficiency under ATE Debug Time Constraints
Young-Woo Lee, Inhyuk Choi, Kang-Hoon Oh, James Jinsoo Ko, and Sungho Kang
Yonsei University and Teradyne Inc.

Date: September 15
Time: 15:20-17:00
Session A5: OSAT Session (Invited)

Location: Room 504a
Session Chair: Daniel Tille

(A5-1)
The Trend of IC Test Industry
Wendy Chen
KYEC

(A5-2)
SiP Integration and Test Challenges
Roger Huang
ASE

(A5-3)
The Challenge to Increase Fault Coverage in IC Testing Process
Herbery Tsai
Chroma ATE Inc.

(A5-4)
A Probe Card Metrology Process Enabling Fast Feedback Loops
Dennis Jansen
NanoFocus

Date: September 15
Time: 15:20-17:00
Session B5: Technical Session - Verification and Fault Tolerance

Location: Room 504b
Session Chair: Tomoo Inoue

(B5-1)
Speeding up Power Verification by Merging Equivalent Power Domains in RTL Design with UPF
**Charles C.-H. Hsu and Charles H.-P. Wen*
National Chiao Tung University

(B5-2)
Assignment for Fault Tolerant Stochastic Computing with Linear Finite State Machines
**Hideyuki Ichihara, Motoi Fukuda, Tsuyoshi Iwagaki, and Tomoo Inoue*
Hiroshima City University

(B5-3)
An Integrated Design Environment of Fault Tolerant Processors with Flexible HW/SW Solutions for Versatile Performance/Cost/Coverage Tradeoffs
**Yi-Ju Ke, Yi-Chieh Chen and Ing-Jer Huang*
National Sun Yat-sen University and Cadence Design Systems

(B5-4)(Invited)
Collaborative Analytics for Back-End Testing
Keith Arnold
PDF Solutions

Date: September 15
Time: 15:20-17:00
Session C5: Embedded Tutorials (Invited)

Location: Room 504c
Session Chair: Chih-Tsun Huang

(C5-1)
At-Speed Test Challenges for Giga-Size and Giga-Hertz Designs
Kun-Han Tsai
Mentor, A Siemens Business

At-speed test is a must to ensure the high quality of today's high performance ICs by screening out timing defects. This tutorial highlight the main challenges for testing today's high performance designs with multiple cores and the state-of-art solutions in industrial designs.

(C5-2)
Deep Neural Network Design and Applications on Testing
Jin-Fu Li
National Central University

Deep neural networks (DNNs) have demonstrated excellent performance on various tasks such as the analytics of image, video, audio, and text. However, DNNs have the nature of highly parallel computing such that they are power-hungry. Therefore, effective low-power design techniques are imperative for the mobile applications. Among various DNN classes, multilayer perceptron (MLP) and convolutional neural network (CNN) are two widely used DNN classes. In this embedded tutorial, we will introduce the concept of MLP and CNN first. Then, low-power design techniques for CNN are described. Finally, possible applications of DNNs on the IC testing are summarized.

(C5-3)
Statistical Soft Error Rate (SSER) for Nanometer Designs
Charles Wen
National Chiao Tung University

n this talk, we re-examine the soft-error effect caused by radiation-induced particles beyond the deep submicron regime. Considering the impact of process variations, voltage pulse widths of transient faults are found no longer monotonically diminishing after propagation, as they were formerly. As a result, the soft error rates in scaled electronic designs escape traditional static analysis and are seriously underestimated. A new concept of statistical soft error rate (SSER) is presented with an analysis framework for coping with the aforementioned concerns. More advanced issues like temperature and aging will be covered if time permits.

General information

Official Language

English is the official language of the conference.

Badge and Admission

All registered participants are required to wear the badges to enter the meeting rooms, exhibition area, social programs and other related events. ITC-Asia badge can access SEMICON Taiwan exhibition.

Registration

ITC-Asia registration counter is located at Room 504abc, 5F, Taipei Nangang Exhibition Center, Hall 1.
Registration hours:
Sep. 13 11:00-17:00
Sep. 14 08:00-17:00
Sep. 15 08:00-13:00

Free WiFi Access

Free WiFi is avaliable in Taipei Nangang Exhibition Center, Hall 1. Please connect "TWTC Free" to access.

Lunch Gathering Location

Lunch gathering is located at ITC-Asia exhibition in I area, 1F, Taipei Nangang Exhibition Center, Hall 1. Join us with lunch coupon in the conference bag.