The 1st IEEE International Test Conference in Asia (ITC-Asia)

Sept. 13-15, 2017

Technical Program (with Hyperlinks)

Sept. 13 - Wednesday	Sept. 14 - Thursday	Sept. 15 - Friday
Registration	9:00-10:50 Opening & Keynote Session (I) Keynote 1: **Hardware Security - Verification, Test, and Defense Mechanisms** - Tim Cheng (HKUST) Keynote 2: **Convergence of Electronic and Semiconductor Systems, and Its Impact on Testing Technology** - Ishih Tseng (Chroma ATE)	9:00-10:30 Keynote Session (II) Keynote 3: **Seven Major Trends that are Changing how we Test ICs** - Phil Nigh (GlobalFoundries) Keynote 4: **Test Emerging Memories** - Rob Aitken (ARM)
	10:50-11:10 Coffee Break	10:30-11:00 Coffee Break
	11:10-12:30 Plenary Panel Heterogeneous Integration – Design and Test Challenges Organizer and Chair: Cheng-Wen Wu, NTHU	11:00-12:15 Sessions A3, B3, C3 ● A3: (Invited) EDA Session ● B3: Test for InFO and SoC ● C3: Memory Test
	12:30-13:50 Lunch Break	12:15-13:50 Lunch Break
13:30-16:50 Half-Day Tutorials ● Automotive Test ● 3D-IC Test ● Yield Learning	13:50-15:05 Sessions A1, B1, C1 ● A1: (Invited) Corporate Session I ● B1: Analog/Mixed Signal Test ● C1: Cell-Aware Test	13:50-15:05 Sessions A4, B4, C4 ● A4: (Invited) Fabless & IDM Session ● B4: On-Chip Test Infrastructure ● C4: Advanced Test Practices
	15:05-15:20 Coffee Break	14:45-15:00 Coffee Break
	15:20-17:00 Sessions A2, B2, C2 ● A2: (Invited) Corporate Session II ● B2: Detection, Diagnosis, Debug ● C2: Test for IoT and Automotives	15:20-17:00 Sessions A5, B5, C5 ● A5: (Invited) OSAT Session ● B5: Verification & Fault Tolerance ● C5: Embedded Tutorials

Sept. 13 – Wednesday, 13:30-16:50 am
Half-Day Tutorials

Topic 1: Automotive Test Strategies

Speaker: Yervant Zorian

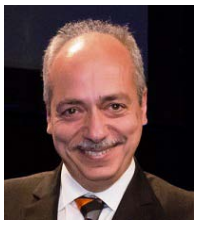
Synopsys

Chair: Shi-Yu Huang

Abstract

Given today's fast growing automotive semiconductor industry, this tutorial will discuss the implications of automotive test, reliability and functional safety requirements on all aspects of the SOC lifecycle: design, silicon bring-up, volume production, and particularly in-system functional safety. Today's automotive safety critical chips need multiple in-system self-test modes, such as power-on self-test and repair, periodic in-field self-test, advanced error correction, etc. This tutorial will cover these specific in-system modes and the benefits of selecting ISO 26262 certified solutions to ensure standardized functional safety requirements, while accelerating time to market for automotive SOCs.

Biography



Dr. Zorian is a Chief Architect and Fellow at Synopsys, as well as President of Synopsys Armenia. Formerly, he was Vice President and Chief Scientist of Virage Logic, Chief Technologist at LogicVision, and a Distinguished Member of Technical Staff AT&T Bell Laboratories. He is currently the President of IEEE Test Technology Technical Council (TTTC), the founder and chair of the IEEE 1500 Standardization Working Group, the Editor-in-Chief Emeritus of the IEEE Design and Test of Computers and an Adjunct Professor at University of British Columbia. He served on the Board of Governors of Computer Society and CEDA, was the Vice President of IEEE Computer Society, and the General Chair of the 50th Design Automation Conference (DAC) and several other symposia and workshops.

Dr. Zorian holds 35 US patents, has authored four books, published over 350 refereed papers and received numerous best paper awards. A Fellow of the IEEE since 1999, Dr. Zorian was the 2005 recipient of the prestigious Industrial Pioneer Award for his contribution to BIST, and the 2006 recipient of the IEEE Hans Karlsson Award for diplomacy. He received the IEEE Distinguished Services Award for leading the TTTC, the IEEE Meritorious Award for outstanding contributions to EDA, and in 2014, the Republic of Armenia's National Medal of Science.

He received an MS degree in Computer Engineering from University of Southern California, a PhD in Electrical Engineering from McGill University, and an MBA from Wharton School of Business, University of Pennsylvania. Back to TOP of the Program

Topic 2: Testing of 2.5D- and 3D-Stacked Integrated Circuits

Speaker: Dr. Erik Jan Marinissen

IMEC – Leuven, Belgium

Chair: Jin-Fu Li

Abstract

After a long period of technology hype, finally real 3D-stacked IC products containing through-silicon vias and micro-bumps (and also their interposer-based 2.5D-SIC variant) are hitting the market. Testing of 2.5D- and 3D-SICs is fraught with new test and design-for-test challenges, for which solutions are only emerging. The test challenges are the following. (1) Test flows: what to test for when? (2) Test content: do these stacked ICs bring new defects and faults and how do we test for those? (3) Test access: how do we pump in/out the test stimuli/responses into the dies and die stacks? In this tutorial, we present the fundamentals of 3D fabrication processes, defects, and fault modeling. We discuss test flows and present test-flow cost modeling and optimization. The tutorial covers the most promising solutions for pre-bond and post-bond (stack) testing, including advances in 3D probe technology, advanced 3D-DfT architectures and optimization, and the ongoing IEEE P1838 standardization effort for test access.

Biography

Erik Jan Marinissen is Principal Scientist at the world-renowned research institute imec in Leuven, Belgium, where he is responsible for the research on test and design-for-test, covering topics as diverse as TSV-based 3D-stacked ICs, silicon photonics, CMOS technology nodes below 10nm, and STT-MRAMs. In addition, he is Visiting Researcher at Eindhoven University of Technology, the Netherlands. Previously, he worked at NXP Semiconductors and Philips Research Laboratories in Eindhoven. Marinissen holds an MSc degree in Computing Science (1990) and a PDEng degree in Software Technology (1992), both from Eindhoven University of Technology. He is (co-)author of 250 journal and conference papers and (co-) inventor on fifteen granted US/EP patent families. Marinissen is recipient of the Most Significant Paper Awards at ITC 2008 and ITC 2010, Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop 1995 and the IEEE International Board Test Workshop 2002, the Most Inspirational Presentation Award at the IEEE Semiconductor Wafer Test Workshop 2013, the HiPEAC Tech Transfer Award 2015, and finalist for the National Instruments' Engineering Impact Award 2017. He served as Editor-in-Chief of IEEE Std 1500 and as Founder and Chair (currently Vice-Chair) of the IEEE Std P1838 Working Group on 3D test access. Marinissen is founder of the workshops 'Diagnostic Services in Network-on-Chips' (DSNOC), DATE's Friday 3D Integration, and the IEEE 'International Workshop on Testing Three-Dimensional Integrated Circuits' (3D-TEST). He has been Program Chair of DDECS 2002, ETS 2006, 3D-TEST 2009-15, and DATE 2013, and General Chair of ETW 2003, DSNOC 2007-08, 3DIW 2009-10, and serves on numerous conference committees, including ATS, DATE, ETS, ITC, ITC-Asia and VTS. He serves on the editorial boards of IEEE 'Design & Test' and Springer's 'Journal of Electronic Testing: Theory and Applications'. During the span of his career, Marinissen has supervised 35 international MSc and PhD students. He is a Fellow of IEEE and Golden Core Member of Computer Society. Marinissen presented numerous tutorials at conferences like 3DIC, 3D-ASIP, ATS, DATE, ETS, ETW, ITC, VTS. Back to TOP of the Program

Topic 3: Industrial Advancements in Diagnosis Driven Yield Analysis

Speakers: Yu Huang, Wu-Yang, and Wu-Tung Cheng

Mentor, A Siemens Business Corp.

Chair: Chien-Mo Li

Abstract

Delivering a stable high yield product on time is the ultimate goal for the semiconductor industry. With the increasing complexity of design and processes, too often, the yield is lower than expected or takes longer to ramp to the target level. Scan diagnosis driven yield analysis (DDYA) can expedite the debug and analysis process reducing the time-to-market and minimizing the related cost. Identifying systematic defects, understanding the root causes of the systematic defect and selecting the right die and suspect candidate for physical failure analysis (PFA) are important components for yield analysis. The recent technology advances in scan chain diagnosis, layout-aware and cell-aware diagnosis can provide fast, high resolution and accurate volume diagnosis data used in the aforementioned steps.

Based on volume diagnosis results, different analysis techniques are developed to help identify the systematic defects. These methodologies include the systematic suspect location analysis, wafer zonal analysis, design-for-manufacturing (DFM) correlation analysis, root-cause deconvolution (RCD) and some others. RCD is a statistical analysis method utilizing Bayesian model. It calculates the defect weight probability with the design information and diagnosis results. It provides a direct or visual defect distribution pareto based on maximum likelihood and further helps drill down to the correspondent die and suspect for each root cause, which can be used for PFA. In this DDYA solution, the PFAs on the selected die and suspect candidates are to validate the findings on the systematic root causes. Hence it greatly reduces the efforts, costs and time for yield analysis. The tutorial will review the recent industrial advancements in the above three areas and each topic will be covered for about 50 minutes.

Biography

Wu-Tung Cheng (S'84–M'85–SM'90–F'00) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1978 and 1982, respectively, and the Ph.D. degree in computer science from the University of Illinois at Urbana–Champaign, Urbana, IL, in 1985. From 1985 to 1990, he was with AT&T Bell Laboratories, Princeton, NJ, developing a test pattern generation system for digital circuits. From 1990 to 1993, he was a cofounder of CheckLogic System, Inc., and was the Vice President of Engineering, leading a team to develop commercial automatic test-generation products, which included FastScan, FlexTest, and DFTAdvisor. In 1993, CheckLogic was merged with Mentor, A Siemens Business Corporation, Wilsonville, OR. Since then, he has had various technical and management positions in design for test area at Mentor, A Siemens Business Corporation. He is currently a Chief Scientist and the director of Advanced Test Research, leading a team to develop new design-for-test solutions for future semiconductor quality and yield issues. He has published over 120 research papers in these areas and is the Coinventor of 30 patents. Dr. Cheng serves as a member of several technical program committees of workshops and conferences.

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Dr. Yu Huang is a Principal Engineer in Mentor, A Siemens Business. He holds 13 US patents and has 9 patents pending. He has published more than 100 papers on leading IEEE Journals, conferences and workshops. He is a senior member of the IEEE. He has served as technical program committee member for DAC, ITC, ATS, ETS, ASPDAC, NATW and some other conferences and workshops in the testing area.

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Sept. 14 – Thursday, 9:00-10:40 am
Keynote Session (I)

Keynote 1:

9:00-9:45am, Sept. 14

Hardware Security - Verification, Test, and Defense Mechanisms

Speaker: Prof. Tim Cheng

Hong Kong U. of Science and Technology

Abstract

In this talk I will illustrate several types of Hardware Trojans and security threats they create, as well as opportunities of Trojan insertion in all steps of the design, fabrication, and testing processes. I will then discuss their defense mechanisms, verification techniques for Trojan detection and prevention, and test-specific need and challenges for hardware security.

Biography

K.-T. Tim Cheng received his Ph.D. in EECS from the University of California, Berkeley in 1988. He has been serving as Dean of Engineering and Chair Professor of ECE and CSE at Hong Kong University of Science and Technology (HKUST) since May 2016. He worked at Bell Laboratories from 1988 to 1993 and joined the faculty at Univ. of California, Santa Barbara in 1993 where he was the founding director of UCSB's Computer Engineering Program (1999-2002), Chair of the ECE Department (2005-2008) and Associate Vice Chancellor for Research (2013-2016). His current research interests include hardware verification and security, design automation for photonics IC and flexible hybrid circuits, memristive memories, mobile embedded systems, and mobile computer vision. He has published more than 400 technical papers, co-authored five books, adviced 40+ PhD theses, and holds 12 U.S. Patents in these areas.

Cheng, an IEEE fellow, received 10+ Best Paper Awards from various IEEE and ACM conferences and journals. He has also received UCSB College of Engineering Outstanding Teaching Faculty Award. He served as Editor-in-Chief of IEEE Design and Test of Computers and was a board member of IEEE Council of Electronic Design Automation's Board of Governors and IEEE Computer Society's Publication Board.

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Keynote 2:

Convergence of Electronic and Semiconductor Systems, and Its Impact on Testing Technology

Speaker: Ishih Tseng

Chroma ATE Inc.

Abstract

As electronic systems are increasingly dominated by system ICs, convergence of electronic system test and semiconductor test is now essential. Environmental variances and stresses often plays vital role in yield or reliability of both system IC and electronic systems. Testing system variables on ICs can significantly enhance reliability of final systems, but also becomes one of major testing challenges for IC vendors. Electronic system also comprises multiple physical interfaces, like optical light, mechanical vibration, temperature, or even chemical contents. Such integration is now migrated upstream into semiconductor process or substrate process. Semiconductor test is no longer just digital or analog test. Integration of wide variety of measurement instruments also pose tremendous challenges not only to test equipment vendors, also to manufacturing operators. The effort and challenges in those two areas will be discussed, primarily from equipment vendor point of view.

Biography

Dr. I-Shih Tseng is the President of Chroma ATE Inc. He joined Chroma in 1998 and involved in the development of semiconductor test equipment. Other positions I-shih served at Chroma including Deputy Chief Engineer, Research Vice President, Semiconductor Test Equipment Business Unit President, Chief Technology Officer, and President of Integrated System Solution BU. Particularly in semiconductor test solution, Chroma provides VLSI test system, SoC/analog test system, system/final level tri-temp test handler, and PXI/PXIe IC test platform. He is also the Chairman of ADIVIC Corporation. I-Shih received his Ph.D. in mechanical engineering from The Pennsylvania State University, Penn., and B.S. from National Taiwan University. His technical expertise includes semiconductor testing system, system automation, and mechanical engineering.

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Sept. 15 – Thursday, 9:00-10:30 am

Keynote Session (II)

Session Chair: (TBD)

Keynote 3:

Seven Major Trends that are Changing how we Test ICs

Speaker: Phil Nigh

GlobalFoundries

Abstract

Products such as mobile processors, Automotive ICs, 5G ICs and the slowdown of technology scaling are changing how we perform development & production testing. In this talk, I'll summarize the 7 trends driving change – and describe how the test industry must change given these emerging requirements.

- ***Automotive ICs*** *– achieving extreme Quality & Reliability & Cost requirements while enabling online, continuous testing in the field. (including advanced fault models, test coverage metrics and analytical methods)*
- ***Multichip Products*** *(such as 2.5D and MCMs) – industry-wide Test collaboration is required to achieve the vision of the Heterogeneous Integration Industry Roadmap (integrating KGD/bare die from multiple suppliers)*
- ***E2E Data Analytics Collaboration*** *– enabling Adaptive Testing (for cost & quality) and cross-company analytics for Test optimization (including OSAT data feedforward & analytic methods)*
- ***5G/mmWave/RF/Silicon Photonics*** *– we need robust, flexible production test capability instead of point solutions*
- ***Technology scaling is driving decreased performance margins*** *– requiring different test approaches and design resilience for long-term field reliability*
- ***Rapid time-to-volume*** *– IC testing now has a major role in driving fab & design learning (e.g., yield) – production testing methods need to significantly improve to enable faster yield ramping*
- ***Component System-level Testing*** *(SLT) – should we be driving to avoid SLT … or embrace it? How does ATE production testing change if we accept SLT is required?*

Biography

Dr. Phil Nigh is a Distinguished Member of Technical Staff and has been a Test Engineer for over 34 years at IBM and GLOBALFOUNDRIES and is responsible for defining & driving Test Strategy including test methods, design-for-test, diagnostic methods and Adaptive Testing. Phil received his PhD from Carnegie Mellon University in 1990. Phil received the Best Paper award at the International Test Conference in 1999 and has done a number of keynote addresses at conferences and workshops and has over 40 world-wide patents. He has organized the "Industry Test Challenges" workshop for over 15 years.

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Keynote 4

Topic: Test Emerging Memories

Speaker: Robert Aitken

ARM Research

Abstract

As device scaling slows down, memories are among the hardest hit circuits. Bit cell dimensions push the limits of design rules, and dense structures make achieving high yields difficult, even with the regularity of memory structures. The workhorse memories of the last twenty years, SRAM, DRAM and NAND flash are all facing significant challenges going forward. While the dominant technologies have struggled, some radically new memory technologies have been proposed to take their place. This talk looks at what these technologies are and where they fit within the memory hierarchy, but also looks at their test implications: What failure modes are likely? How can a resistive crosspoint be tested? What redundancy and repair methods make sense and what yield issues can they cover? Answering these questions is key to commercial success for emerging memories, but the answers are different enough that some of our intuition about memory test will need replacing in order to reflect a new reality.

Biography

Rob Aitken is an ARM Fellow responsible for technology direction at ARM Research. He works on low power design, technology roadmapping, and next generation memories. He has worked on 15+ Moore's law nodes and has published over 80 technical papers, on a wide range of topics. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He holds a Ph.D. from McGill University in Canada. Dr. Aitken is an IEEE Fellow, and serves on a number of conference and workshop committees.

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Sept. 14 – Thursday, 11:00-12:20 am

Plenary Panel

Organizer and Moderator: Prof. Cheng-Wen Wu

Topic: Heterogeneous Integration – Design and Test Challenges

It is of utmost importance to smart handheld devices and many advanced IOT applications that we should continue to improve the power efficiency and reduce the cost of a system, and for such system to obtain both high data bandwidth and high system performance in a small form factor. As Moore's Law is slowing down, advanced heterogeneous 3D and 2.5D integration is gradually taking over the key role for that purpose. However, there are design and test challenges that we need to deal with. In this panel, we invite expert panelists to address and discuss challenges, potential solutions, and cases from different angles of view. The panel will also give comparisons among SOC, SiP, MCM, PoP, InFO, 3D-IC, etc. The audience are welcome to interact with the panelists by giving comments and asking questions.

Panelists:

- *Jason Hsu, MediaTek*
- *Edward Lee, RealTek*
- *Yervant Zorian, Synopsys*
- *Roger Hwang, ASE*
- *Erik Jan Marinissen, IMEC*
- *Shih-Lien Lu, TSMC*

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Sept. 14 – Thursday, 13:30-14:45 pm

Session A1: (Invited) Corporate Session (I)

Session Chair: Seiji Kajihara

A1-1

The Trend of Testing on IoT Ics

**George Chang,* Chroma ATE Inc., Taiwan

ICs have been widely used for IoT applications in network and sensor layers. To ensure the function, performance and quality of each IC to meet required standard becomes critical. There are many key test items and variables to be implemented during testing, including thermal, RF, accuracy, speed, and etc. In this tutorial, we will introduce advanced semiconductor test solutions, including VLSI test system, SoC/analog test system, system/final level IC test handler, PXI/PXIe IC test platform, laser diode test system for wireless, MCU, PMIC, and sensor applications.

A1-2

Economic Trade-off in Probe Card Solutions

**Daniel Chen,* Japan Electronic Materials Corporation, Taiwan

Advanced vertical fine pitch probe cards can compete economically with traditional , low cost cantilever probe cards. They have more touch-down life, little need for mid-life realignment, less tester/prober down time.

A1-3

Improved Test Quality and Efficiency Via Better Link of Design and Test

**Meir Gellis,* Test Insight Ltd., Israel

In 1993 the Pentium processor had 3.1 million transistors, less than 20 years later by 2012 Intel's 3rd Generation Core processor had 1.4 billion. Today, even mixed signal devices come with serious amounts of logic including hundreds of registers that require setting (and modifying) during validation and test.
Over the years a greater use of scan test has helped cope with increasing complexity and Test Engineers do a remarkable job keeping up with ever increasing demands - despite the basic flow for creating a new test program having remained much the same – essentially, use a skeleton program and paste new

tests/patterns etc. and then debug.

The above, introduce great challenges in quality and efficiency to semiconductors test engineers. More sophisticated software solutions can help addressing those challenges by a more automated flow as well as better verification methodologies. TestInsight has been in this market since 1999 providing the state of the art software solutions in the traditional test development environment, and is now leading the effort to more automation and better quality assurance in the new challenging design methodologies.

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Sept. 14 – Thursday, 13:30-14:45 pm

Session B1: Analog and Mixed-Signal Test

Session Chair: Soon-Jyh Chang

B1-1: **Low-Distortion Signal Generation for Analog/Mixed-Signal Circuit Testing with Digital ATE**

*Masayuki Kawabata, Koji Asami, Shohei Shibuya, *Tomonori Yanagida and Haruo Kobayashi*

B1-2: **A Quick Jitter Tolerance Estimation Technique for Bang-bang CDRs**

**Yen-Long Lee and Soon-Jyh Chang*

B1-3: **Evaluation of Loop Transfer Function Based Dynamic Testing of LDOs**

Mehmet Ince, Sule Ozev, Ender Yilmaz, Jae Woong Jeong and Leroy Winemberg

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Sept. 14 – Thursday, 13:30-14:45 pm

Session C1: Cell-Aware Test

Session Chair: Martin Keim

C1-1: (invited) **The Role of Test in Advanced System Design – Challenges & Opportunities**

**Yin Wang,* Cadence

C1-2: **Test Generation for Open and Delay Faults in CMOS Circuits**

**Cheng-Hung Wu, Kuen-Jong Lee and Sudhakar M. Reddy,* National Cheng-Kung Univ., Taiwan

C1-3: **Cell-Aware Test Generation Time Reduction by Using Switch-Level ATPG**

**Po-Yao Chuang, Cheng-Wen Wu and Harry H. Chen,* National Tsing Hua Univ., Taiwan

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Sept. 14 – Thursday, 15:00-16:40 pm
Session A2: (Invited) Corporate Session (II)
Session Chair: Mango (Chia-Tso) Chao

A2-1

Cadence Modus Test Solution,

**Yin Wang,* Cadence Design Systems, Taiwan

Cadence digital and signoff tools have undergone a fundamental revolution and have changed how semiconductor system designs are done today. This past year, Cadence launched their new DFT, ATPG, and Diagnostics tool: Modus. The key benefit to users is a patented new test compression technology which can reduce test time up to 3X and elegantly solves the routing congestion issues caused by traditional XOR based compression.

A2-2

Silicon test solutions for giga-gate SOC designs and automotive ICs

**Wu Yang,* Mentor, A Siemens Business, USA

The advanced technology nodes of nowadays enable the unprecedented giga-gate size SOC designs. This brings in new challenge for IC test in the area of test data volume, time-to-market, computation resource, pin count and silicon learning. The automotive IC in its own market has an extra layer of complexity and challenge for test. These ICs must meet strict standards and operate under extreme conditions with wild swings in voltages, electrostatic discharge and long life span. People are looking for scalable, integrated and proven test solutions to address the challenges. This session will give a high level overview on comprehensive test solutions Mentor, A Siemens Business, can bring to you and the value.

A2-3

Improved ON-resistance Measurement at Wafer Probe using "DARUMA" stage of ACCRETECH UF2000

**Yuichi Kakizaki,*TESEC Corporation, Japan

Low ON resistance in MOSFET test was required only after packaging. It is now required at front wafer

probe test process to guarantee its characteristics for wafer sales. However, technical challenge lies in wafer test as it requires longer test time compared to final test by conventional method. The longer test time brings other negative effects. It is not only lower output but instability of test result due to increased temperature at NP junction or chip stress. Tesec would like to introduce current discrete testing trend and propose a new system solution for Low ON resistance wafer test with Accretech prober of DARUMA stage.

A2-4

Testing Modern Devices with Modern Tools

*Hau Lam, Test Systems Strategies, Inc., USA

The complexity in modern devices pushes design and test engineers to communicate cross functionally and integrate methodologies in different stages of a device development cycle.

To compete with the cheapest product offering with the shortest time-to-market in the consumer market, or to ensure zero-defect requirement in the medical and automotive sectors, different components such as RF, Low-power management, analog instrumentation, the latest DFT strategies, and 2.5D/3D-stacks all need to be tested in concert.

This presentation describes TSSI's modern test program generation and validation software tool refined over 38 years of serving the semiconductor industry.

Modern tools must automate digital pattern generation, mixed-signal program generation and validation pre-silicon for the design team, and post-silicon for the test team, all using the same easy-to-use tool environment. Plus, data retention in a robust and intelligent way is key in this tool for cross-discipline tool integration for yield improvement processes.

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Sept. 14 – Thursday, 15:00-16:40 pm

Session B2: Detection, Diagnosis, and Debugging

Session Chair: Tong-Yu Hsieh

B2-1: **GPU Accelerated Fault Dictionary Generation for the TRAX Fault Model**

Matthew Beckler and **Shawn Blanton,* Carnegie Mellon Univ., USA

B2-2: **Physical-aware Diagnosis of Multiple Interconnect Defects**

*Jing-Yu Chen, Po-Hao Chen, Chi-Lin Lee, *Po-Wei Chen, and Chien-Mo Li,* National Taiwan Univ., Taiwan

B2-3: **A Run-Pause-Resume Silicon Debug Technique for Multiple Clock Domain Systems**

**Shuo-Lian Hong and Kuen-Jong Lee,* National Cheng-Kung Univ., Taiwan

B2-4: **A Hybrid Concurrent Error Detection Scheme for Simultaneous Improvement on Probability of Detection and Diagnosability**

**Chih-Hao Wang and Tong-Yu Hsieh,* National Sun Yat-Sen Univ., Taiwan

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Sept. 14 – Thursday, 15:00-16:40 pm

Session C2: Test for IoT and Automotives

Session Chair: Charles H.-P. Wen

C2-1: **A Dependable AMR Sensor System for Automotive Applications**

*Andreina Zambrano and *Hans Kerkhoff*

C2-2: **An Automotive MP-SoC Featuring an Advanced Embedded Instrument Infrastructure for High Dependability**

**Hans G. Kerkhoff, Ghazanfar Ali, Hassan Ebrahimi, and Ahmed Ibrahim*

C2-3: **Symbiotic System Models for Efficient IOT System Design and Test**

**Cheng-Wen Wu, Bing-Yang Lin, Hsin-Wei Hung, Shu-Mei Tseng, and Chi Chen*

C2-4: **A Lightweight X-Masking Scheme for IoT-Designs**

**Daniel Tille, Benedikt Gottinger, and Ulrike Pfannkuchen*

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Sept. 15 – Friday, 10:50-12:05 am
Session A3: (Invited) EDA Session
Session Chair: Jiun-Lang Huang

A3-1: The Emerging Applications of Machine Learning in Testing

**Yu Huang, Mentor, A Siemens Business*

Machine learning has already been applied in different fields of EDA. In the testing area, it has been applied in data mining for yield learning, root cause analysis for years. Some recent research has applied it to test scheduling and DFT planning. In the near future, we will see more research and development of its applications in diagnosis or even ATPG. In this talk, we will discuss the machine learning applications in testing and predict its trending.

A3-2: Integrated Electrical and Thermal Analysis flow for Integrated Fan-Out(InFO) Wafer Level Package

**Charlie Shih, Cadence Design Systems*

In this presentation, we'll introduce an integrated power network analysis flow with static and dynamic IR drop analysis and layer-based electro-migration (EM) violation analysis, in which an IC package layout database can be directly included in the analysis flow so that the design hotspot can be identified entirely from chip to package design. An electrical package performance assessment(EPA) capability in IC package layout integrated with electrical analysis engine is introduced to perform electrical rule checking during the design implementation stage. A complete signal integrity(SI) and power integrity (PI) analysis in time domain for high-speed serial link and parallel bus simulation and electro-magnetic interference (EMI) in frequency domain is proposed based on 3D fullwave s-parameter model extraction including chip and package designs. A thermal aware electro-migration (EM) analysis flow enabled by a layout-based power consumption and temperature map file is proposed to perform chip-package-PCB thermal co-analysis.

A3-3: Moving Test to RTL for High Testability, Functional Safety and Reliability

**Dmitry Melnik, Synopsys*

This talk will cover general test violation analysis, physically-aware test points to maximize testability and achieve highest possible ATPG and LBIST coverage, and top-level DFT connectivity validation challenges. An exciting, additional area covered is soft error analysis which is required by the ISO 26262 automotive functional safety requirements for design tolerance.

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Sept. 15 – Friday, 10:50-12:05 am

Session B3: Test for InFO and SoC

Session Chair: Hans Tsai

B3-1: **Fan-Out Wafer Level Chip Scale Package Testing**

**Hao Chen, Hung-Chih Lin, and Min-Jer Wang*

B3-2: **Testing-for-Manufacturing (TFM) for Ultra-thin IPD on InFO**

**Tang-Jung Chiu*

B3-3: (invited) **Test Strategy for Storage SoCs**

*Abhishek Bhattacharya and *Ramesh Tekumalla*

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Sept. 15 – Friday, 10:50-12:05 am

Session C3: Memory Test

Session Chair: Shyue-Kung Lu

C3-1: **Adaptive Block-Based Refresh Techniques for Mitigation of Data Retention Faults and Reduction of Refresh Power**

**Shyue-Kung Lu*

C3-2: **Software-Hardware-Cooperated Built-In Self-Test Scheme for Channel-Based DRAMs**

**Tsung-Fu Hsieh, Jin-Fu Li, Kuan-Te Wu, Jenn-Shiang Lai, Chih-Yen Lo, Ding-Ming Kwai, and Yung-Fa Chou*

C3-3: **Adapting an Industrial Memory BIST solution for testing CAMs**

*Jais Abraham, Uttam Garg, Glenn Colon-Bonet, Ramesh Sharma, Chennian Di, Benoit Nadeau-Dostie, Etienne Racine, and *Martin Keim*

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Sept. 15 – Friday, 13:30-14:45 pm

Session A4: (Invited) Fabless and IDM Session

Session Chair: Harry Chen

A4-1: (invited) **DFT Challenges and Solutions for Automotive ICs**

**Ying-Yen Chen,* RealTek Semiconductor Corp, Taiwan

Abstract—Compared to consumer ICs, automotive ICs have more stringent requirement including extremely high test coverage, short failure analysis time and the ability of in-field test and diagnosis. In this presentation, we will describe the challenges we faced and the solutions we took in DFT aspect of automotive ICs.

A4-2: (invited) **Multi-Pronged Strategy to Reduce Scan Test Cost at Advanced Process Nodes**

**Jianguo Ren,* MediaTek Inc., Taiwan

Abstract: For advanced semiconductor processes, more and more fault models are required to improve chip quality, causing a dramatic rise in scan-related production test cost. We can address test cost reduction at three levels: design planning, chip implementation, and ATE execution. This talk will focus on chip implementation and ATE execution: (1) circuit modifications to increase scan shift frequency, and (2) constraining ATE timing sets to be speed-path and IR-drop aware. Adoption of these solutions has resulted in a 50% reduction of scan-related test cost across many products at MediaTek.

A4-3: (invited) **What do we do to make system reliable?**

**Xinli Gu*, Huawei Technologies, USA

Abstract

A reliable system requires an end-to-end planning, design, manufacturing test and maintenance for reliability. The reliability challenges for a large system come from the followings: 1) new designs and technologies which haven't been fully tested in the field, 2) extremely large number of pieces of designs that no single individual can fully understand its reliability coverage, 3) 3rd party or legacy designs/parts used in the system, and 4) complicated system operation environment in customer field. This presentation will cover the reliability challenges and the best industrial practice, and promote research to work on the methodology for industrial system reliability.

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Sept. 15 – Friday, 13:30-14:45 pm

Session B4: On-Chip Test Infrastructure

Session Chair: Hans Kerkhoff

B4-1: **Trustworthy Reconfigurable Access to On-Chip Infrastructure**
*Michael Kochte, *Rafal Baranowski, and Hans-Joachim Wunderlich*

B4-2: **On the Effects of Real Time and Contiguous Measurement with a Digital Temperature and Voltage sensor**
**Yousuke Miyake, Yasuo Sato, and Seiji Kajihara*

B4-3: **Enhancing Security of Logic Encryption Using Embedded Key Generation Unit**
**Rajit Karmakar, Santanu Chattopadhyay, and Rohit Kapur*

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Sept. 15 – Friday, 13:30-14:45 pm

Session C4: Advanced Test Practices

Session Chair: Ramesh Tekumalla

C4-1: **A Mathematical Model to assess the influence of parallelism in a Semiconductor Back-End Test Floor**

*Davide Appello, Mariapina Laurino, and *Marco Pranzo*

C4-2: **A Fully Automatic Test System for Characterizing Large-Array Fine-Pitch Micro-Bump Probe Cards**

**Erik Jan Marinissen, Ferenc Fodor, Bart De Wachter, Joerg Kiesewetter, Eric Hill, and Ken Smith*

C4-3: **Test Item Priority Estimation for High Parallel Test Efficiency under ATE Debug Time Constraints**

**Young-Woo Lee, Inhyuk Choi, Kang-Hoon Oh, James Jinsoo Ko, and Sungho Kang*

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Sept. 15 – Friday, 15:00-16:40 pm
Session A5: (Invited) OSAT Session
Session Chair: Daniel.Tille@infineon.com

A5-1: (invited) **The Trend of IC Test Industry**

**Wendy Chen*, KYEC, Taiwan

A variety of innovative testing technologies had been developed to solve the testing issues of upcoming advanced devices in different novel applications such as IOX, Smart Living, Healthcare, Automobile, etc. However, not all of the innovative testing technologies can be adopted and applied to large-volume mass production successfully. There are several key factors and hidden burdens that need to be considered and removed. In this talk, practical IC test issues and challenges will be addressed and the trend of IC test industry will be discussed when we look back to the history and foresee the way to the paradise of next generation testing manufactory in the future.

A5-2: (invited) **SiP Integration and Test Challenges**

**Roger Hwang*, ASE, Taiwan

A5-3: (invited) **The Challenge to Increase Fault Coverage in IC Testing Process**

**Herbert Tsai*, Chroma ATE Inc., Taiwan

Due to consumer electronics, automobile and semiconductor products getting higher density, it is necessary to increase fault coverage to guarantee the reliability of final product. The SLT and BI testing play an important role in IC testing process that can provide test data in short term to increase fault coverage. There are many technical challenges in SLT and BI testing that must be managed to implement test process.

A5-4: (invited) **A Probe Card Metrology Process Enabling Fast Feedback Loops**

**Dennis Jansen*, NanoFocus, Germany

A fast probe card inspection process to determine geometric parameters of probe cards such as diameters, shape, co-planarity and position of probe tips as well as orientation, tilt and warp of probe heads in respect to the main board and the probe tips. The process is

designed to provide information about the clearance condition or the condition of the overdrive area, respectively, to early identify such conditions which may damage or destroy wafers during the probing process. The process target was defined to enable an all-over acquisition of probe cards at a wafer test site to judge the general usability or defectiveness of a probe card before or after each single operation as well as to continuously provide detailed wear and tear information about a probe card to the point of its EOL.

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Sept. 15 – Friday, 15:00-16:40 pm

Session B5: Verification and Fault Tolerance

Session Chair: Tomoo Inoue

B5-1: **Speeding up Power Verification by Merging Equivalent Power Domains in RTL Design with UPF**
**Charles C.-H. Hsu and Charles H.-P. Wen*

B5-2: **Assignment for Fault Tolerant Stochastic Computing with Linear Finite State Machines**
**Hideyuki Ichihara, Motoi Fukuda, Tsuyoshi Iwagaki and Tomoo Inoue*

B5-3: **An Integrated Design Environment of Fault Tolerant Processors with Flexible HW/SW Solutions for Versatile Performance/Cost/Coverage Tradeoffs**
**Yi-Ju Ke, Yi-Chieh Chen and Ing-Jer Huang*

B5-4: *(Invited)* **Collaborative Analytics for Back-end Testing**
**Keith Arnold*

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Sept. 15 – Friday, 15:00-16:30 pm
Session C5: Embedded Tutorials
Session Chair: Chih-Tsun Huang

C5-1: At-Speed Test Challenges for Giga-Size and Giga-Hertz Designs
**Kun-Han (Hans) Tsai,* Mentor, A Siemens Business, USA

Abstract: *At-speed test is a must to ensure the high quality of today's high performance ICs by screening out timing defects. This tutorial highlight the main challenges for testing today's high performance designs with multiple cores and the state-of-art solutions in industrial designs.*

C5-2: Deep Neural Network Design and Applications on Testing
**Jin-Fu Li,* National Central Univ., Taiwan

Abstract*: Deep neural networks (DNNs) have demonstrated excellent performance on various tasks such as the analytics of image, video, audio, and text. However, DNNs have the nature of highly parallel computing such that they are power-hungry. Therefore, effective low-power design techniques are imperative for the mobile applications. Among various DNN classes, multilayer perceptron (MLP) and convolutional neural network (CNN) are two widely used DNN classes. In this embedded tutorial, we will introduce the concept of MLP and CNN first. Then, low-power design techniques for CNN are described. Finally, possible applications of DNNs on the IC testing are summarized.*

C5-3: Statistical Soft Error Rate (SSER) for Nanometer Designs
**Charles Wen,* National Chiao-Tung Univ., Taiwan

Abstract*: In this talk, we re-examine the soft-error effect caused by radiation-induced particles beyond the deep submicron regime. Considering the impact of process variations, voltage pulse widths of transient faults are found no longer monotonically diminishing after propagation, as they were formerly. As a result, the soft error rates in scaled electronic designs escape traditional static analysis and are seriously underestimated. A new concept of statistical soft error rate (SSER) is presented with an analysis framework for coping with the aforementioned concerns. More advanced issues like temperature and aging will be covered if time permits.*

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