The 1st Int'l Test Conference in Asia, 2017

(ITC-Asia 2017)

September 13-15, 2017

CO-LOCATED with SEMICON Taiwan

Taipei, Taiwan

http://windy.ee.nthu.edu.tw/ITC-Asia-2017

Steering Committee Members
Gordon Roberts
McGill Univ.

Cheng-Wen Wu
National Tsing Hua Univ.

Yervant Zorian
Synopsys

General Chairs
Kuen-Jong Lee
National Cheng Kung Univ.
Li-C. Wang
U. of California, Santa Barbara

Technical Program Chair
Shi-Yu Huang
National Tsing Hua Univ.

Finance Chair
Chih-Tsun Huang
National Tsing Hua Univ.

Publicity Chair
Min-Der Hsieh
National Cheng Kung Univ.

Publications Chair
Soon-Jyh Chang
National Cheng Kung Univ.

Tutorials Chair
Chien-Mo Li
National Taiwan Univ.

Local Arrangements Chair
Marvis Wu
SEMI Taiwan

Industry Sessions Chair
Harry Chen
MediaTek Inc.

Exhibitions Chair
Terry Tsao
SEMI Taiwan

US Liaison
Krishnendu Chakrabarty
Duke University

Europe Liaison
Hans-Joachim Wunderlich
Stuttgart University

ITC Liaison
Bill Eklow

Contact Information
Program Chair
Shi-Yu Huang
e-mail: syhuang@ee.nthu.edu.tw
Tel: +886-926-681536

Call For Papers

(Outstanding papers with extension will be invited to ITC'17)

With the test technology facing its grand challenges to ensure the quality of ICs and electronic systems incorporating more and more sophisticated manufacturing processes and system integration technologies in various emerging applications such as Internet of Things, cloud computing, automotive electronics, etc., global proliferation and cooperation is increasingly more important. International Test Conference has been a flagship conference in test technology since 1970. With an attempt to stimulate more discussion and interaction between the academia and the industry around the globe, ITC-Asia was initiated and co-located with SEMICON Taiwan in Taipei. Attendee can involve themselves in not only the state-of-the-art test technology trend, but also numerous semiconductor industry forums organized by SEMICON Taiwan.

Topics of Interests include (but are not limited to) the following topics:

Special Promotion: Validation/Debug, Security/Trust, Test Standards for Auto-Electronics

- Design Validation and Debug
- Hardware Oriented Security and Thrust
- ATE Design
- Analog and Mixed-Signal Test
- RF Test
- High-Speed I/O Test
- Fault Modeling and Simulation
- ATPG (Automatic Test Pattern Generation)
- Design for Testability for Logic Circuits
- Built-In Self-Test for Logic Circuits
- Delay Test
- System-on-Chip Test
- Test Compression
- Test Methods for Low-Power Circuits
- Power-Aware and/or Thermal-Aware Test
- Memory Test, Diagnosis, and Repair
- Fault Diagnosis and Failure Analysis
- Test Methods for Emerging Devices
- MEMS Test
- Sensor Test
- CPU/GPU Test
- Automotive IC Test
- Test Methods for Internet of Things
- Online Test
- On-Chip Measurement
- Reliability Issues
- SiP, 2.5D, and 3D IC Test
- Interconnect Test
- Test Standards
- Test Economics
- Fault Tolerance
- Reconfigurable System Test
- Board-Level Testing and Diagnosis
- Yield Analysis and Learning

Submission: (via the conference website)

Regular paper submissions should be made electronically by PDF manuscripts only, not exceeding 6 pages in IEEE 2-column format (including abstract, figures, tables, and bibliography). A submission will be considered evidence that upon acceptance at least one author will attend the conference to make the presentation. Authors of accepted papers are also responsible for preparing the final manuscripts in time to be included in the electronic proceedings, which will eventually be published in *IEEE Xplore* Digital Library. At least one registration to the conference is required for each accepted paper.

Key Dates

- ~~**Submission of title and abstract:** **Feb. 5, 2017**~~ **(extended)**
- **Paper submission:** **Feb. 22, 2017 (extended)**
- **Notification of acceptance:** **April 17, 2017**
- **Camera-ready manuscript:** **June 5, 2017**