Rigorous Test Flow for PLL using Jitter Measurement with VDD Sweeping

以變換電壓之下的抖動量測量為基礎的鎖相迴路嚴格測試方法

Student: 李奕萱 (Yi-Hsuan Lee)

Advisor: 黃錫瑜 教授 (Prof. Shi-Yu Huang)

國立清華大學 NATIONAL TSING HUA UNIVERSITY

IC-Design Exploration Lab

Department of Electrical Engineering

National TsingHua University, HsinChu, Taiwan

Outline

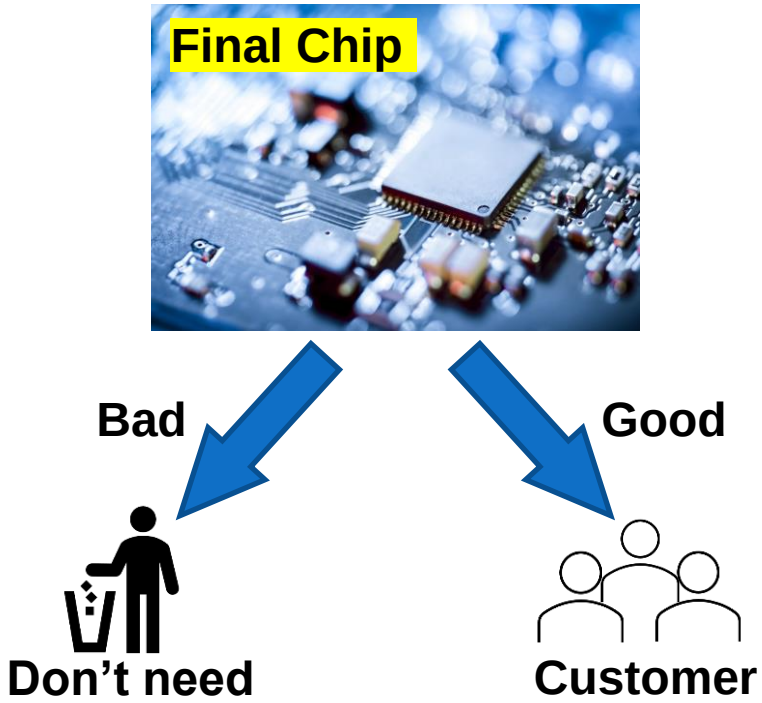
- Introduction
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- Experimental Results
- Conclusion

Outline

- **Introduction**
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- Experimental Results
- Conclusion

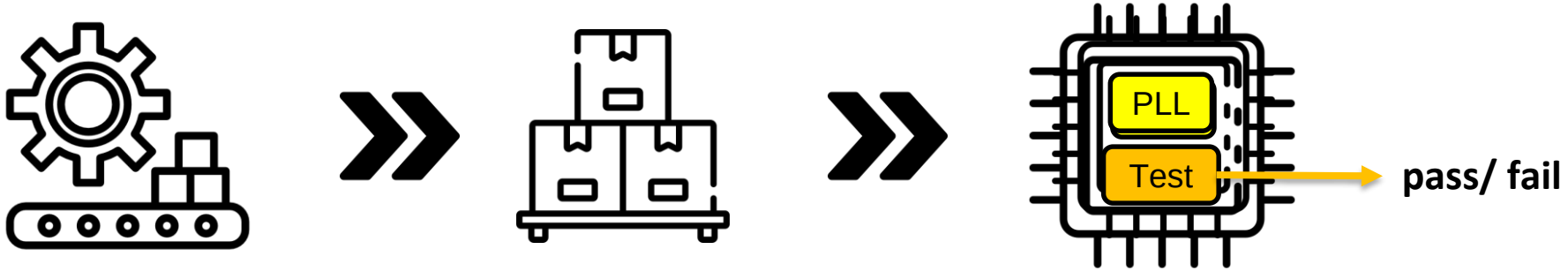
Introduction

- **Verify Manufacturing of Circuit:**
  - System Reliability ↑
  - System Cost ↓
  - Testing Time ↓
  - Cost of Repair after Manufacturing ↓
  - Circuit quality ↑



Rigorous Built-in PLL Test

Why we need Rigorous Built-in Test Flow?

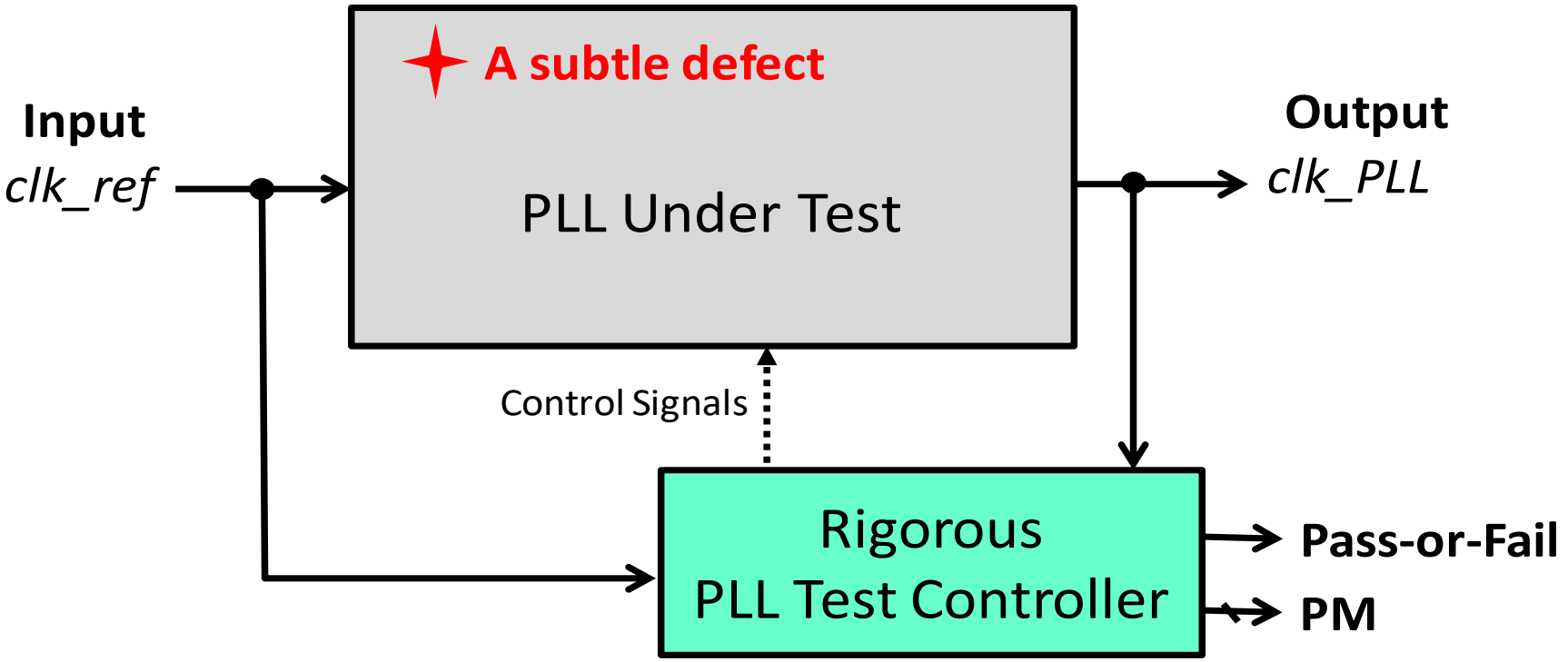


Why we need Rigorous Built-in Test Flow?

Phase-Locked Loop (PLL) → Output Clock

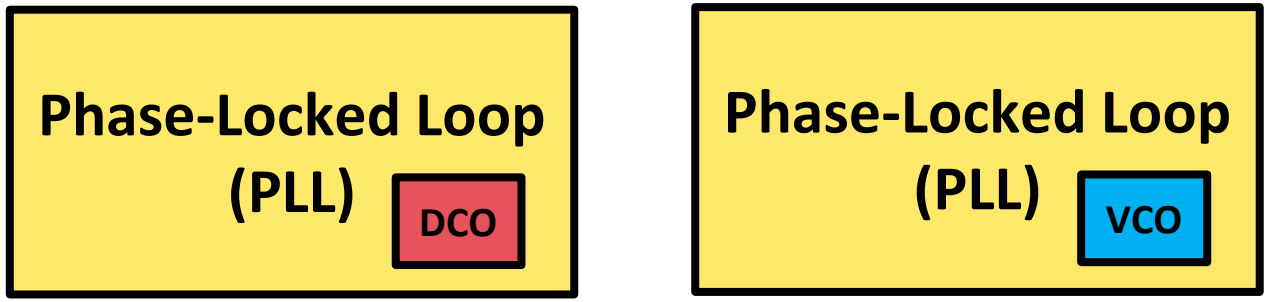
- Hard Fault? Ex: Can't Oscillate.
- Weak Device? At extreme operating conditions.

A functional test setup for a PLL device

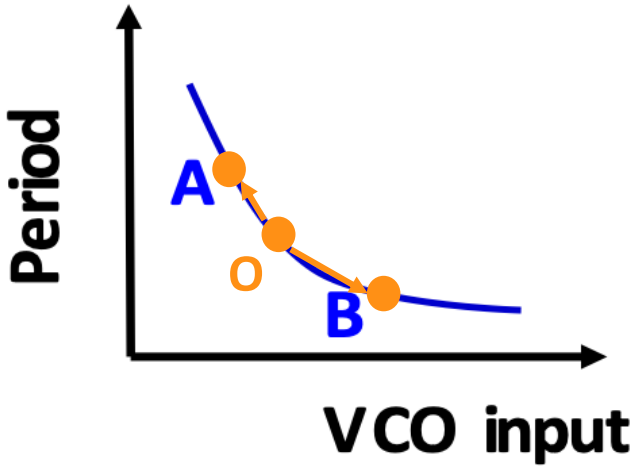


"PM" denotes for Performance Metrics,
Including frequency error and peak-to-peak jitters, etc.

VDD Sweeping



Digitally-Controlled Oscillator Voltage-Controlled Oscillator



- Why we need Jitter Measurement with VDD Sweeping?
  - Temperature may be different
  - → To cover the possible operating range
  - ~~Thermal chamber~~ → Temperature-to-VDD-mapping Scheme

Jitter Measurement

- Under-sampling Method [11][12][13][14]
- Self-referenced TDC Method [15]
- Sampling-based TDC Method [16][17]

[11]S. Sunter and A. Roy, "On-Chip Digital Jitter Measurement, from Megahertz to Gigahertz," *IEEE Design & Test of Computers*, July-Aug., pp. 314-321, 2004.
[12]S. Sunter and A. Roy, "Purely Digital BIST for any PLL or DLL", *Proc. of IEEE European Test Symp*., pp. 1-6, 2007.
[13]R. Kinger, S. Narasimhawsamy, and S. Sunter, "Experiences with Parametric BIST for Production Testing PLLs with Picosecond Precision", *Proc. of IEEE Int'l Test Conf*., pp. 1-9, 2010.
[14]J.-J. Huang and J.-L. Huang, "An Infrastructure IP for On-Chip Clock Jitter Measurement", IEEE Int'l Conf. on Computer Design, pp. 1-6, 2004.
[15]P.-Y. Chou and J.-S. Wang, "An All-Digital On-Chip Peak-to-Peak Jitter Measurement Circuit with Automatic Resolution Calibration for high PVT-Variation Resilience", *IEEE Trans. on Circuits and Systems-I: Regular Papers*, Vol. 66, No. 7, pp. 2508-2518, July 2019.
[16]J. Yu and F. F. Dai, "On-Chip Jitter Measurement Using Vernier Ring Time-to-Digital Converter," *Proc. of Asian Test Symp*., pp. 167-170, 2010.
[17]T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, and A. Inoue, "Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement," *Digest of the Int'l Symp. on VLSI Circuits,* pp. 166-167, June 2008.

Jitter Measurement

- **Under-sampling Method** [11][12]
  - **Indirect Measurement**
  - **Analyze the cumulative distribution of the jitter → RMS jitter**
  - **Highest Resolution**
  - **Extra high-precision crystal oscillator**[13] → **Cost ↑**

[11]S. Sunter and A. Roy, "On-Chip Digital Jitter Measurement, from Megahertz to Gigahertz," *IEEE Design & Test of Computers*, July-Aug., pp. 314-321, 2004.
[12]S. Sunter and A. Roy, "Purely Digital BIST for any PLL or DLL", *Proc. of IEEE European Test Symp.*, pp. 1-6, 2007.
[13]R. Kinger, S. Narasimhawsamy, and S. Sunter, "Experiences with Parametric BIST for Production Testing PLLs with Picosecond Precision", *Proc. of IEEE Int'l Test Conf.*, pp. 1-9, 2010.

Jitter Measurement

- **Under-sampling Method [14]**
  - **Analyze the cumulative distribution of the jitter → RMS jitter**
  - **Two-tap Delay Line → Not a coherent under-sampling clock**
  - **Finite sample size**

[14]J.-J. Huang and J.-L. Huang, “An Infrastructure IP for On-Chip Clock Jitter Measurement”, IEEE Int’l Conf. on Computer Design, pp. 1-6, 2004.

Jitter Measurement

- **Self-referenced TDC Method [15]**
  - **Indirect Measurement**
  - **Measure peak-to-peak jitter**
  - **PLL's output clock signal drive a Delay-Locked Loop**
  - **Period jitter → phase error**
  - **Uncertainty of DLL → measurement error ↑**

[15]P.-Y. Chou and J.-S. Wang, "An All-Digital On-Chip Peak-to-Peak Jitter Measurement Circuit with Automatic Resolution Calibration for high PVT-Variation Resilience", *IEEE Trans. on Circuits and Systems-I: Regular Papers*, Vol. 66, No. 7, pp. 2508-2518, July 2019.

Jitter Measurement

- **Sampling-based TDC Method [16][17]**
  - **Direct Measurement**
  - **Analyze the cumulative distribution of the jitter → RMS jitter**

    → Measure over 100k TDC code. →Time-Consuming

[16]J. Yu and F. F. Dai, "On-Chip Jitter Measurement Using Vernier Ring Time-to-Digital Converter," *Proc. of Asian Test Symp*., pp. 167-170, 2010.
[17]T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, and A. Inoue, "Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement," *Digest of the Int'l Symp. on VLSI Circuits,* pp. 166-167, June 2008.

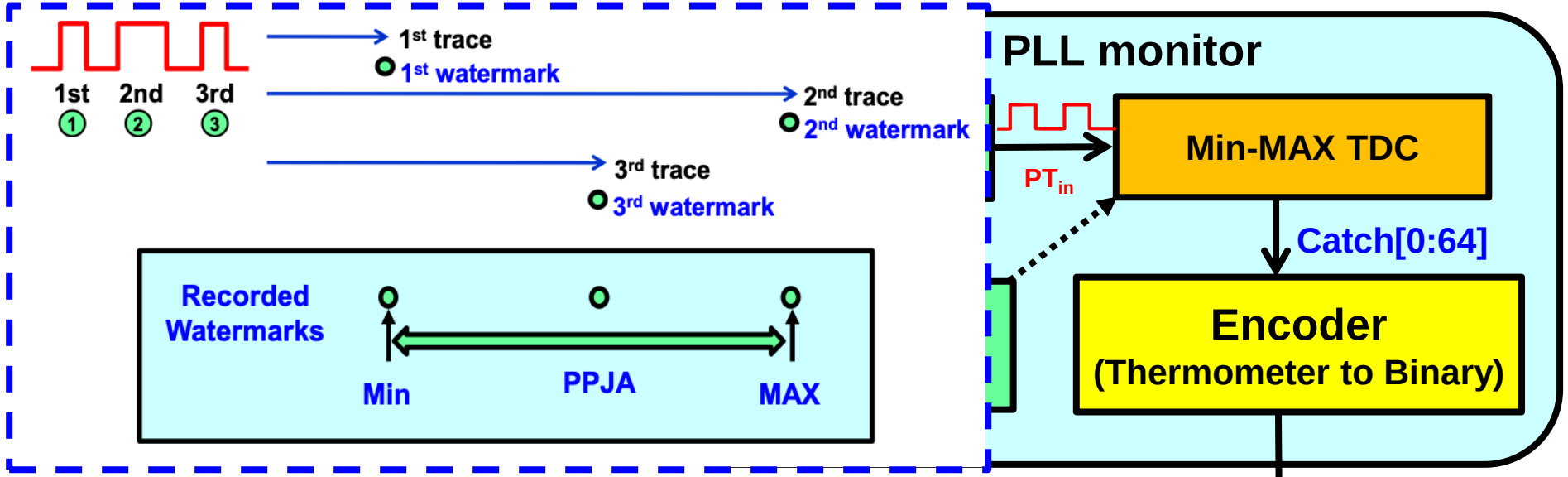
Jitter Measurement

- We use min-Max TDC [24] jitter measurement method.
  - Direct Measurement
  - Measure peak-to-peak jitter
  - Continuously monitor the peak-to-peak jitter → catch short-time glitches
  - On-line jitter validation

- [24] W.-H. Chen, C.-C. Hsu, and S.-Y. Huang, "Rapid PLL Monitoring By a Novel min-MAX Time-to-Digital Converter", Proc. of IEEE Int'l Test Conf., (ITC), pp. 1-8, 2020.

Architecture of PLL Monitor

- **Definition:**
  1) The **min-code** and **Max-code** are the outputs of our PLL monitor and represents the min-period and Max-period, respectively.
  2) **PPJA (Peak-to-Peak Jitter Amount) Code** refer to the difference between min-code and Max-code. It can represent the JJPA.



- [24] W.-H. Chen, C.-C. Hsu, and S.-Y. Huang, "Rapid PLL Monitoring By a Novel min-MAX Time-to-Digital Converter", Proc. of IEEE Int'l Test Conf., (ITC), pp. 1-8, 2020.

Robustness Indicator – PPJA

- PPJA is the “robustness indicator” in this work for weak device detection.

- Reasons why PPJA is a better indicator than the RMS jitter :

	PPJA	RMS jitter
Sensitive	✔	
Catch short-time transient performance hazard	✔	
Performance	worst-case situation or weakness	only the average-case

20ps vs 2ps

Objectives of This Work

- Objectives: More rapid and low cost.
- Through our jitter measurement, we can transfer the PPJA code into the absolute Peak-to-Peak Jitter Amount value in pico-second unit.
- Online validation.
- Classify weak device.
- Built-in PLL test → Prevent dangerous defects before manufacturing.

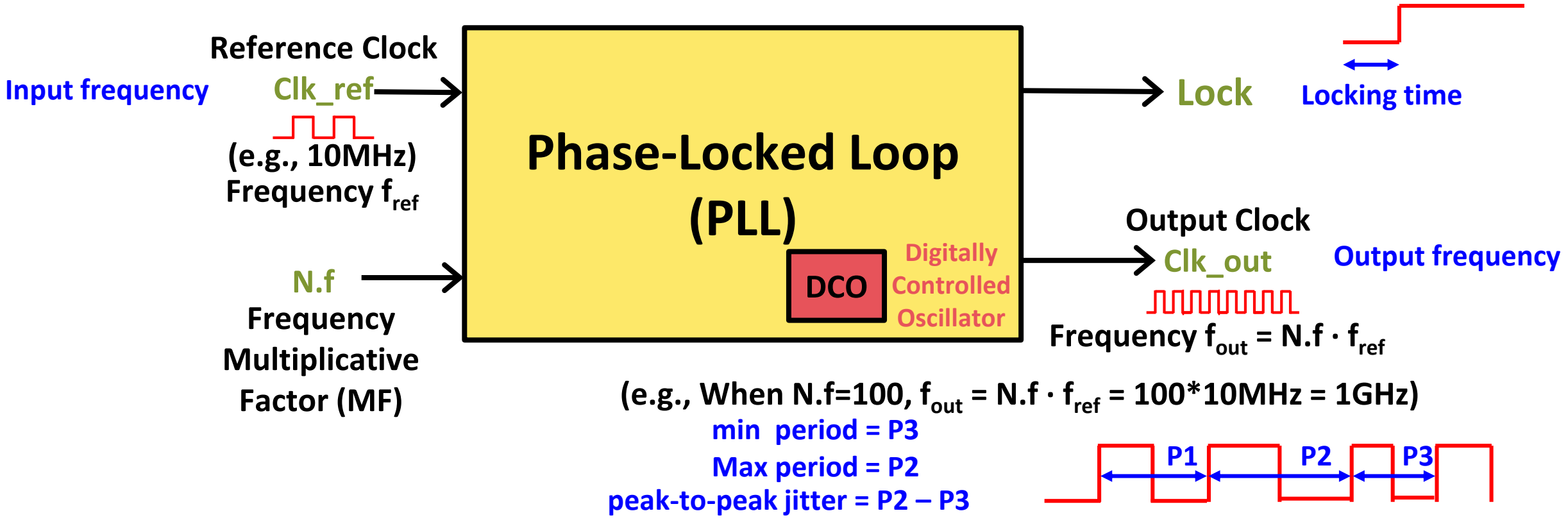
- [24] W.-H. Chen, C.-C. Hsu, and S.-Y. Huang, "Rapid PLL Monitoring By a Novel min-MAX Time-to-Digital Converter", Proc. of IEEE Int'l Test Conf., (ITC), pp. 1-8, 2020.

Outline

- Introduction
- **Proposed Rigorous Test Flow for PLL using Jitter Measurement**
  - **Proposed Jitter Measurement**
  - Proposed Temperature-to-VDD-mapping Scheme
- Experimental Results
- Conclusion

Basic Fractional-N PLL

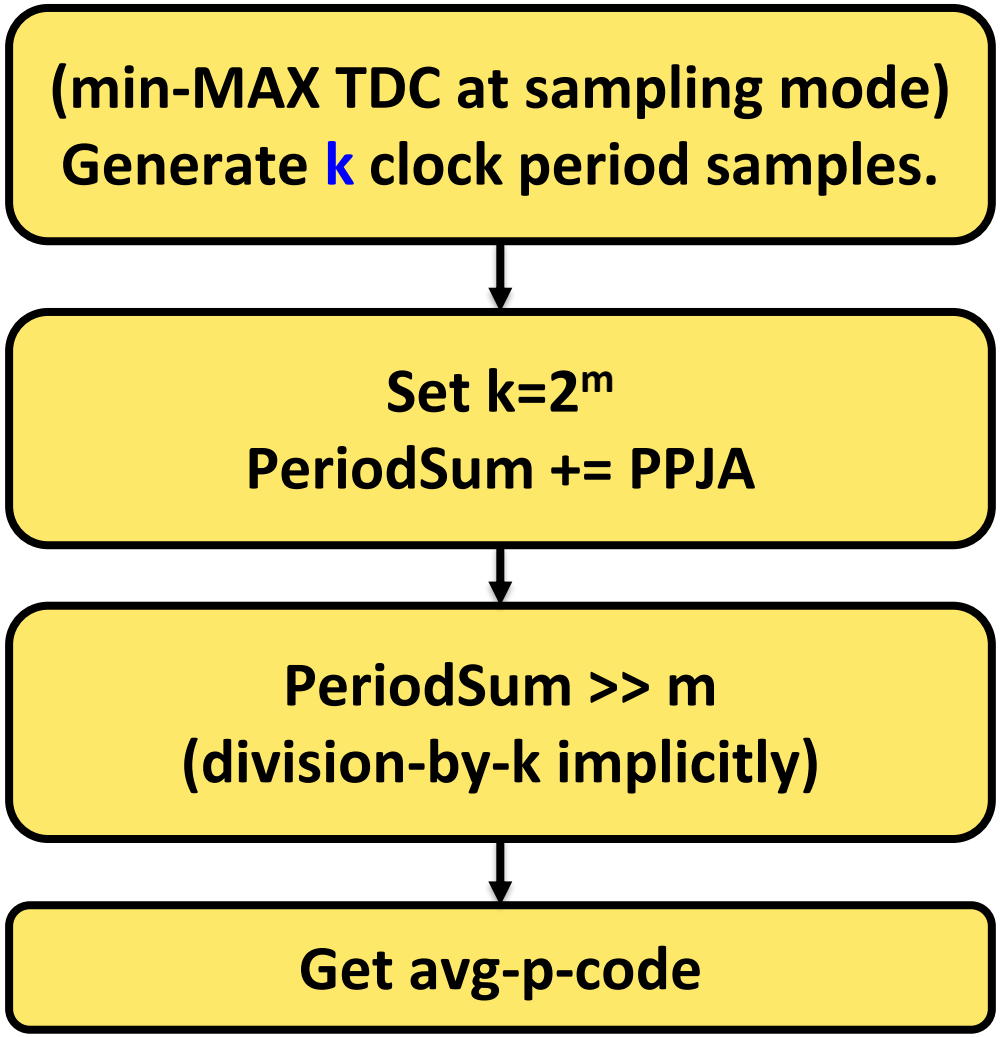
- PLL used as a frequency multiplication circuit to generate high-speed on-chip clock generation. (e.g., 1 GHz clock)



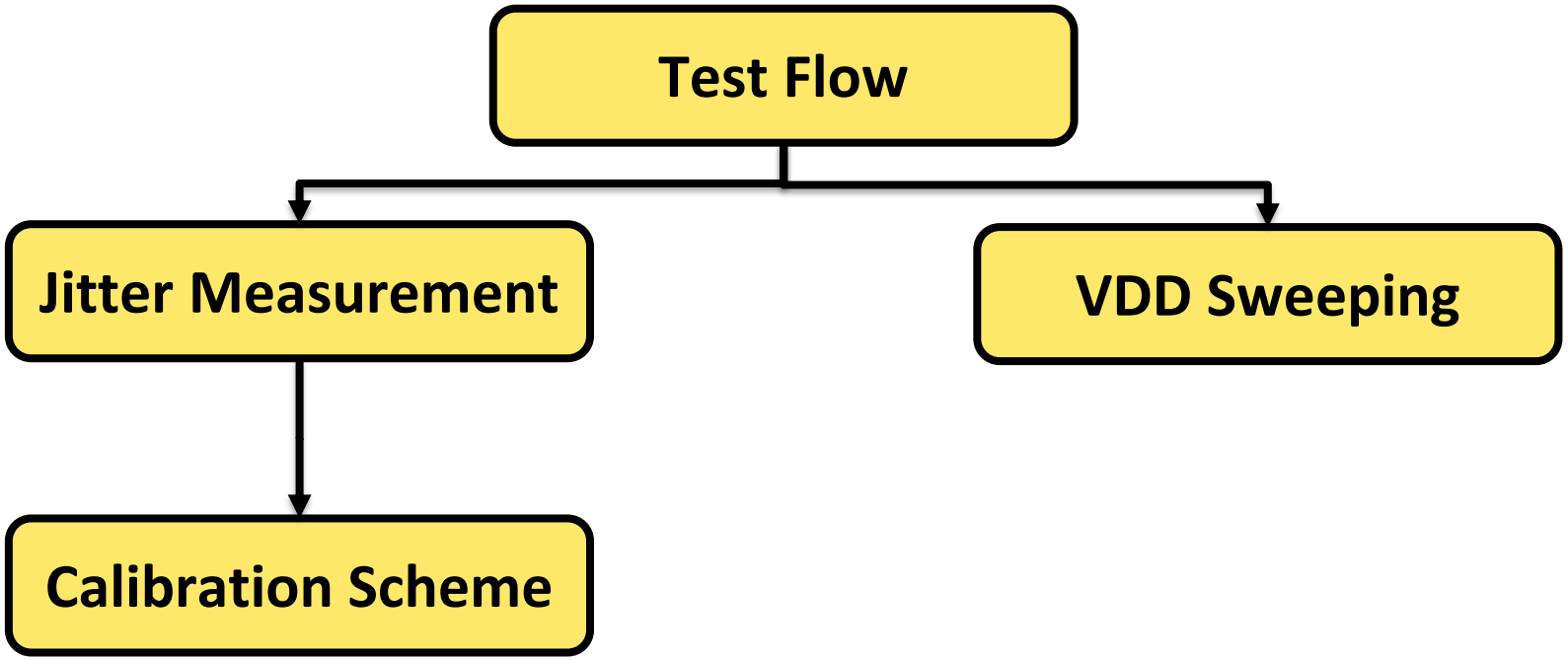
- C.-E. Lee and S.-Y. Huang, "A Cell-Based Fractional-N Phase-Locked Loop Compiler," Proc. of IEEE Int'l Conf. on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD), pp. 273-276, (July 2018).

Implementation

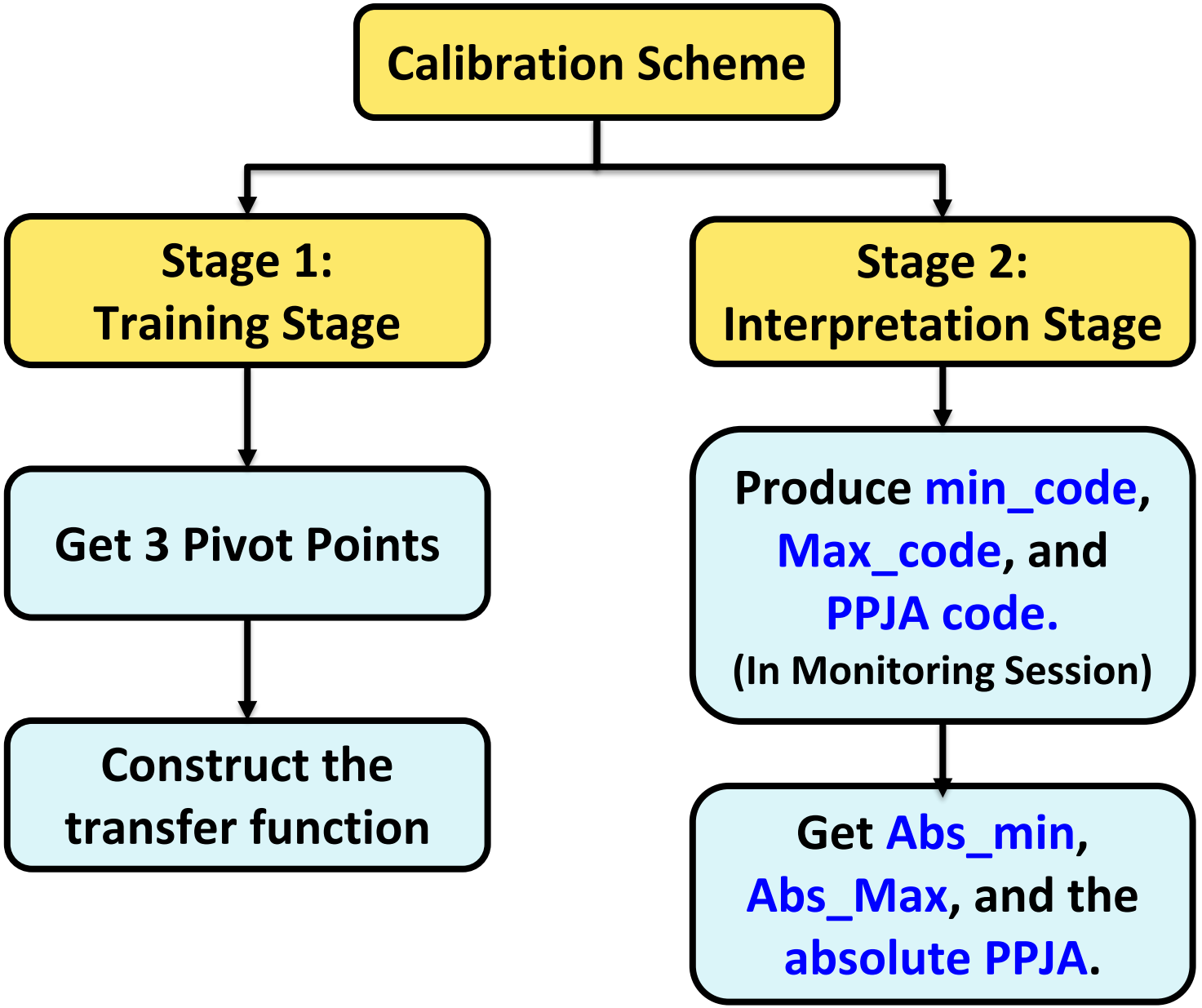
- ✓ **An adder and a simple shifter.**



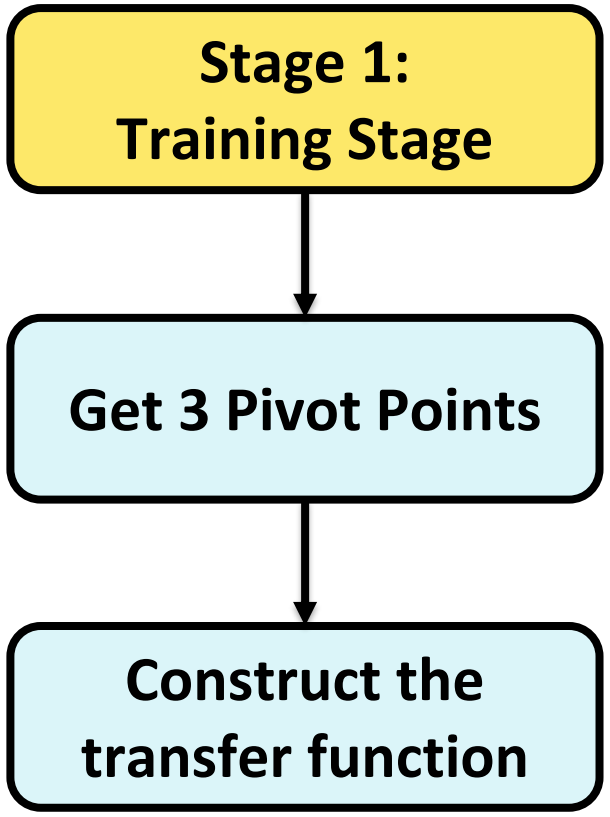
Test Flow

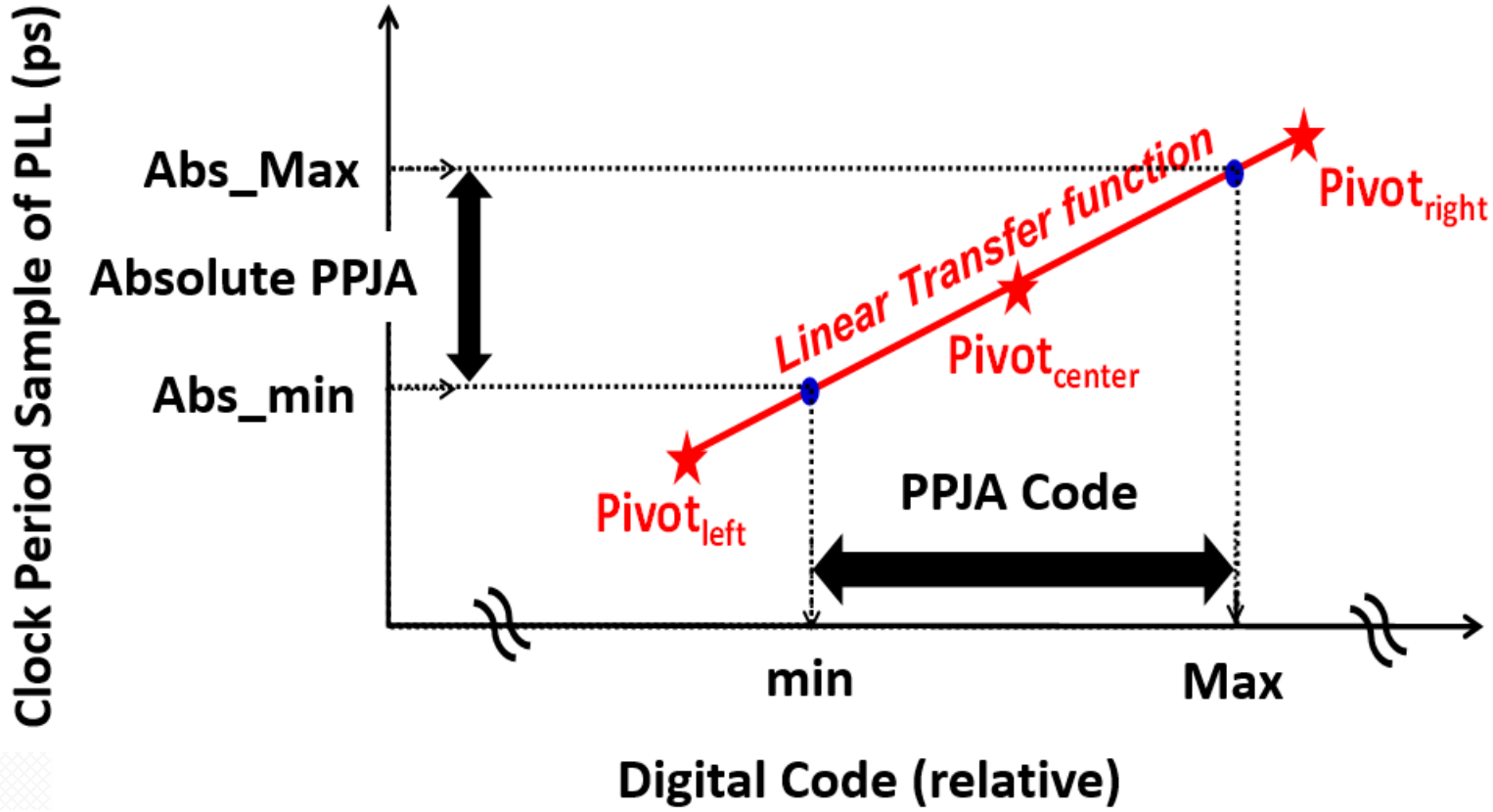

Test Flow
Jitter Measurement
VDD Sweeping
Calibration Scheme

Test Flow


Calibration Scheme
Stage 1:
Training Stage
Get 3 Pivot Points
Construct the transfer function
Stage 2:
Interpretation Stage
Produce min_code, Max_code, and PPJA code.
(In Monitoring Session)
Get Abs_min, Abs_Max, and the absolute PPJA.

Training Stage





Interpretation Stage

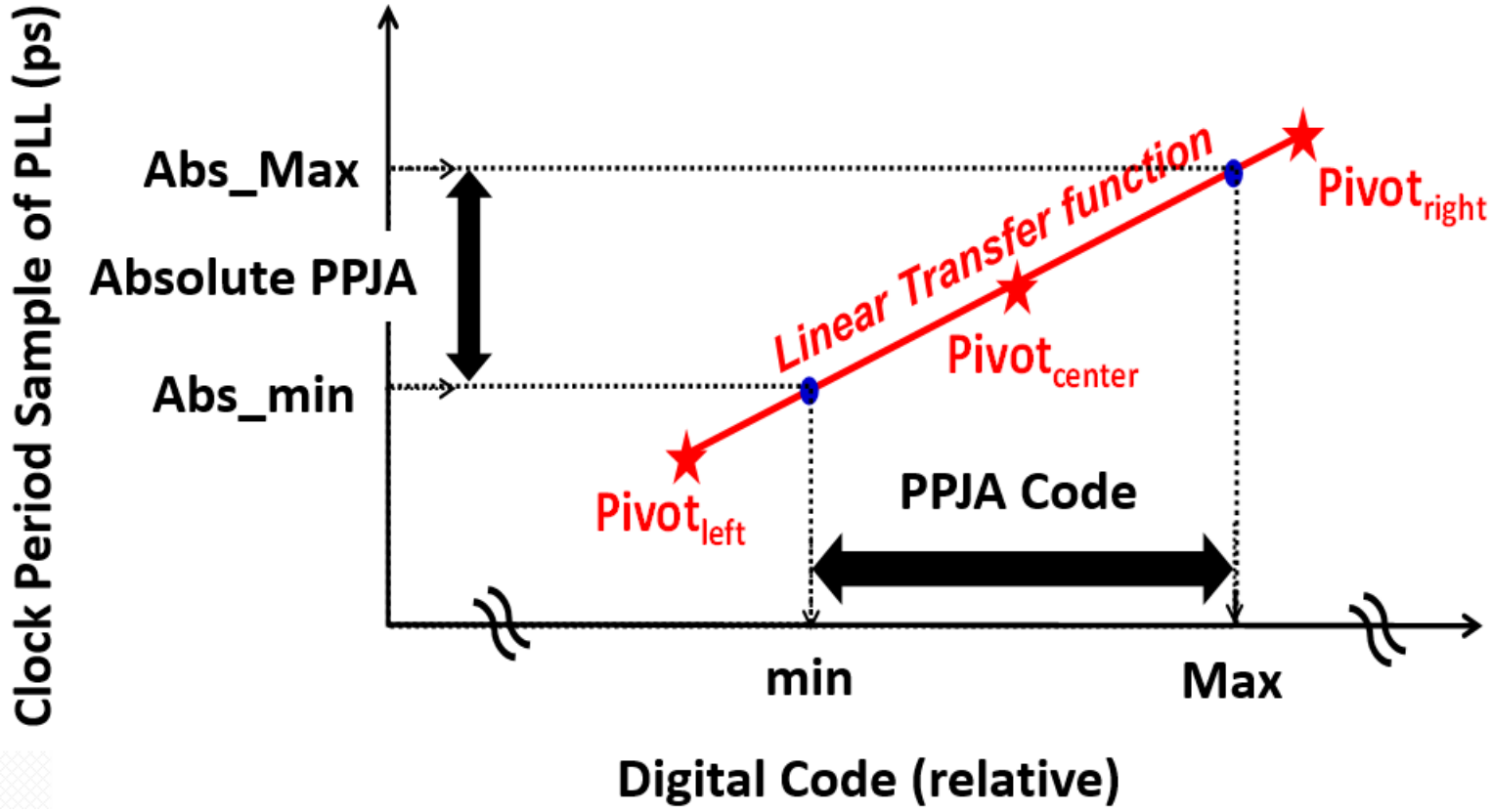
Stage 2: Interpretation Stage

↓

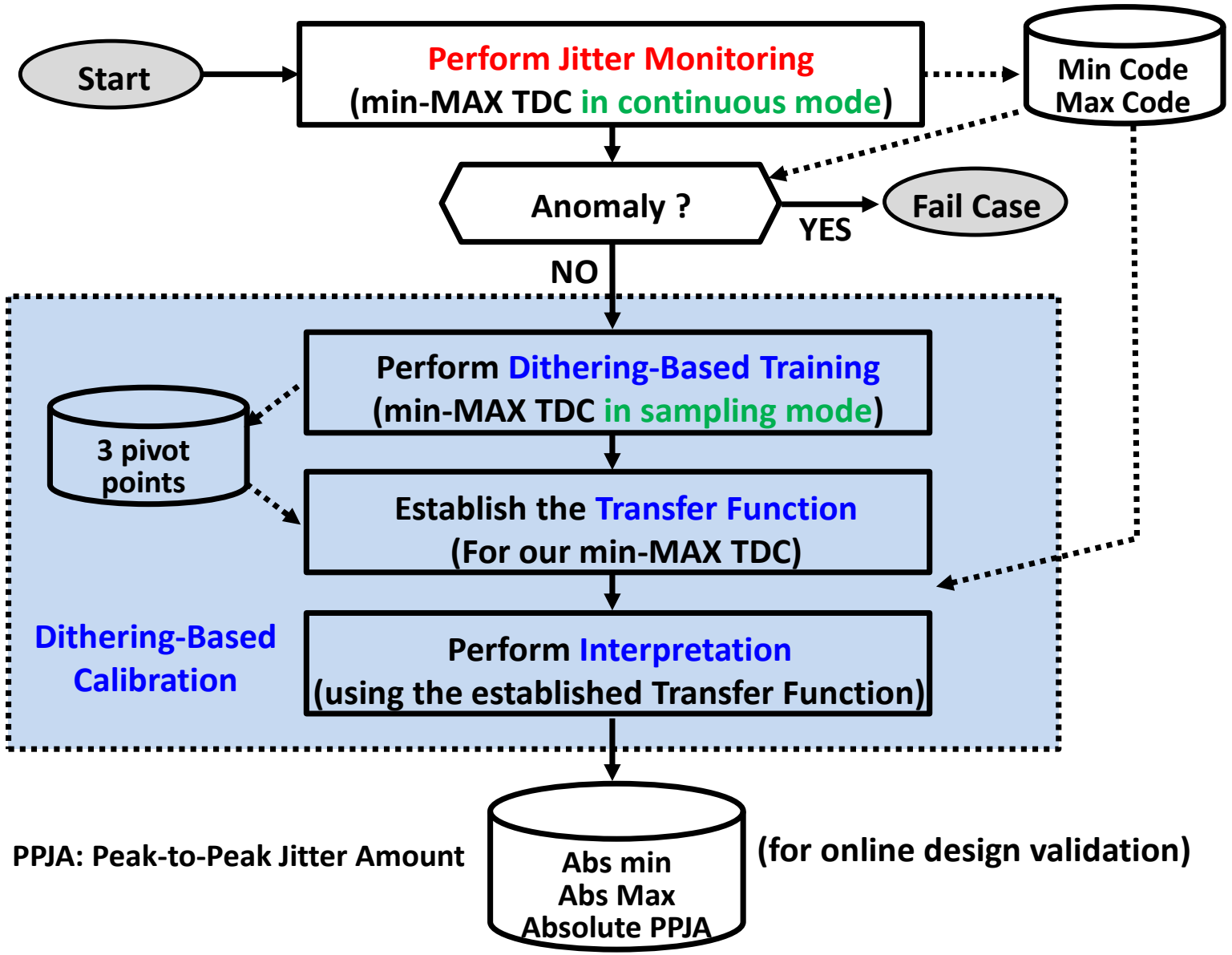
Produce min_code, Max_code, and PPJA code. (In Monitoring Session)

↓

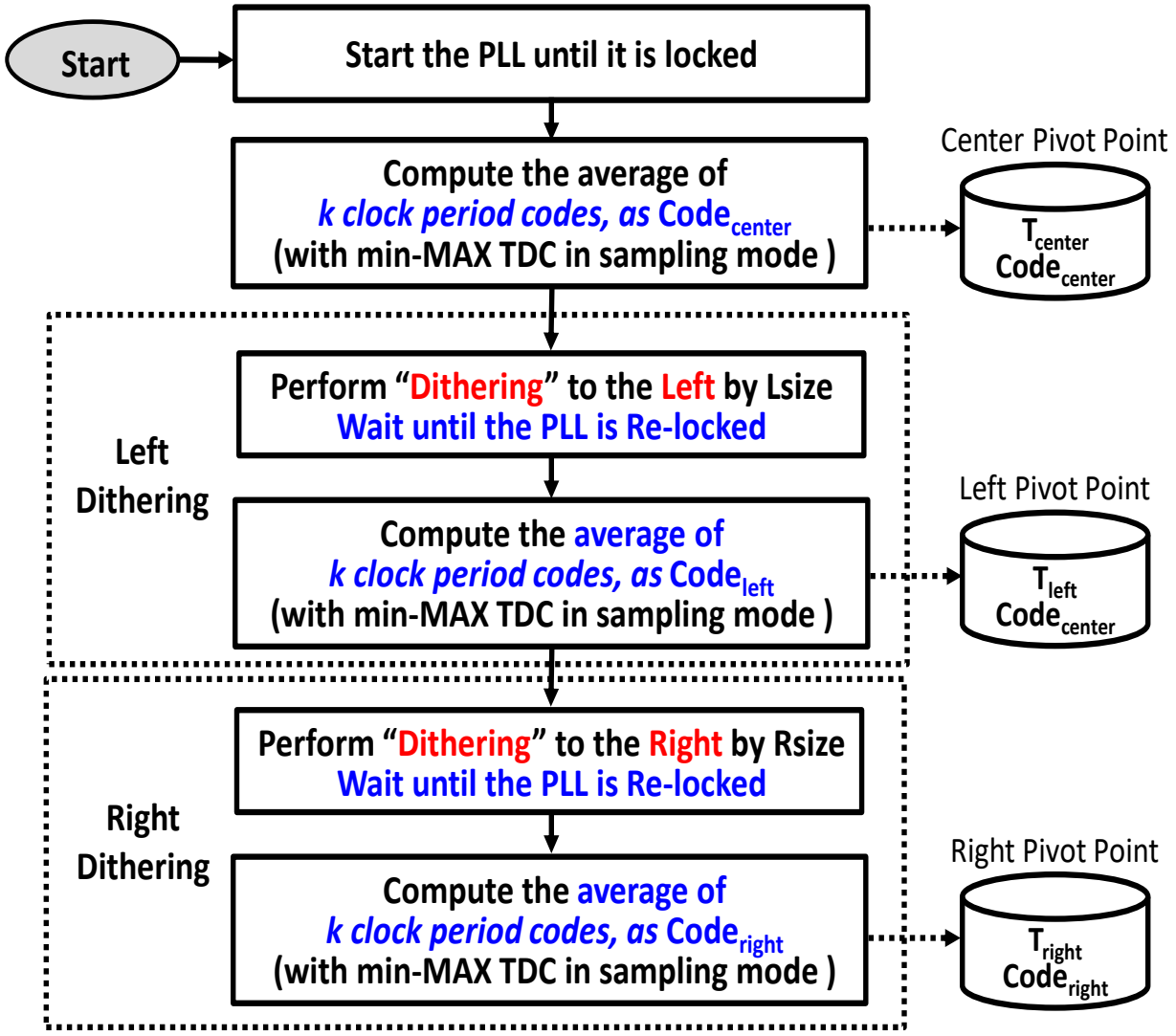
Get Abs_min, Abs_Max, and the absolute PPJA.



Jitter Monitoring and Measurement Flow



Generation of Pivot Points

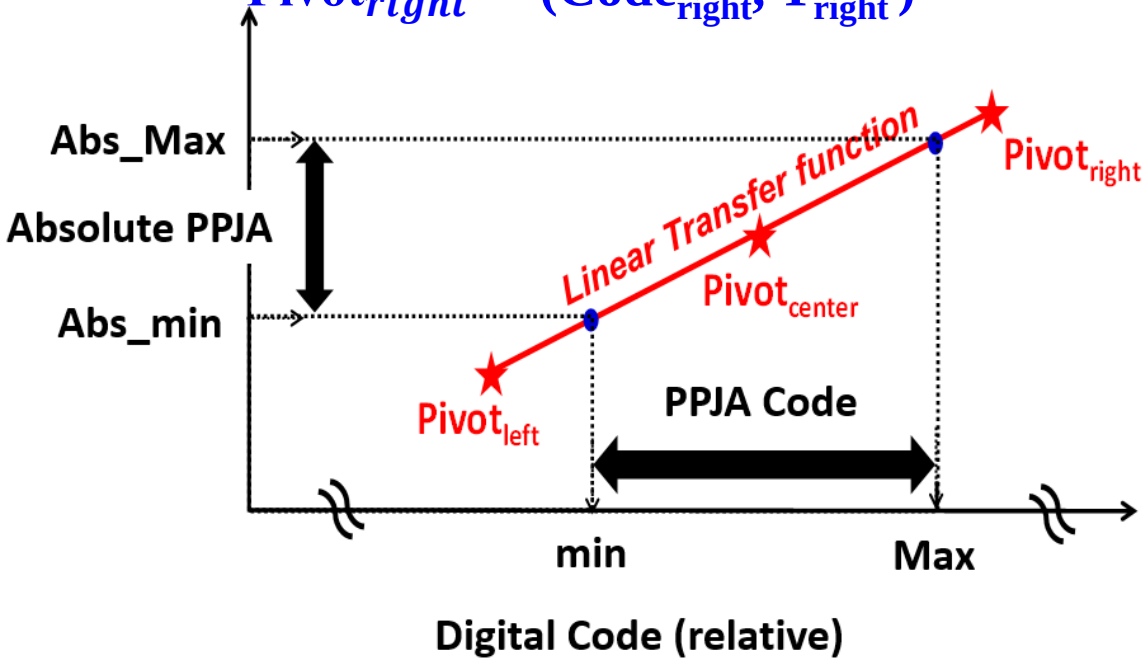


$$Pivot = (x, y)$$

$$Pivot_{center} = (Code_{center}, T_{center})$$

$$T_{right} = T_{center} + R$$
$$T_{left} = T_{center} - L$$

$$Pivot_{left} = (Code_{left}, T_{left})$$
$$Pivot_{right} = (Code_{right}, T_{right})$$



Example

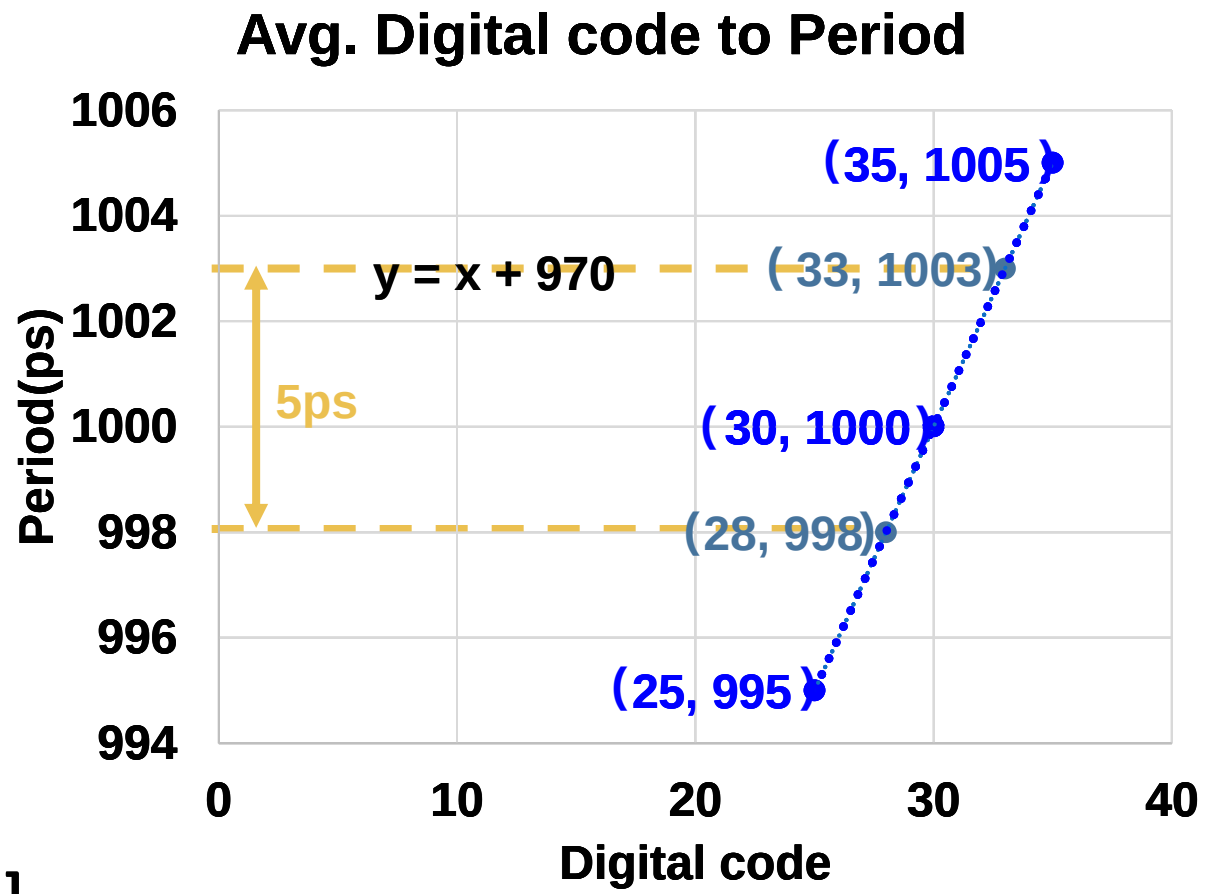
- T_{center} = 1000 ps → $Code_{center}$ = 30
- →$Pivot_{center}$ = (30, 1000)
- Dithering size L = R = 5ps
- → T_{right} = T_{center} + R = 1005ps
- → T_{left} = T_{center} - L = 995ps
- $Code_{right}$ = 35; $Code_{left}$ = 25
- The linear transfer function:

  y = x + 970

- [min-code, Max-code] = [28, 33]

  ↓ y = x + 970

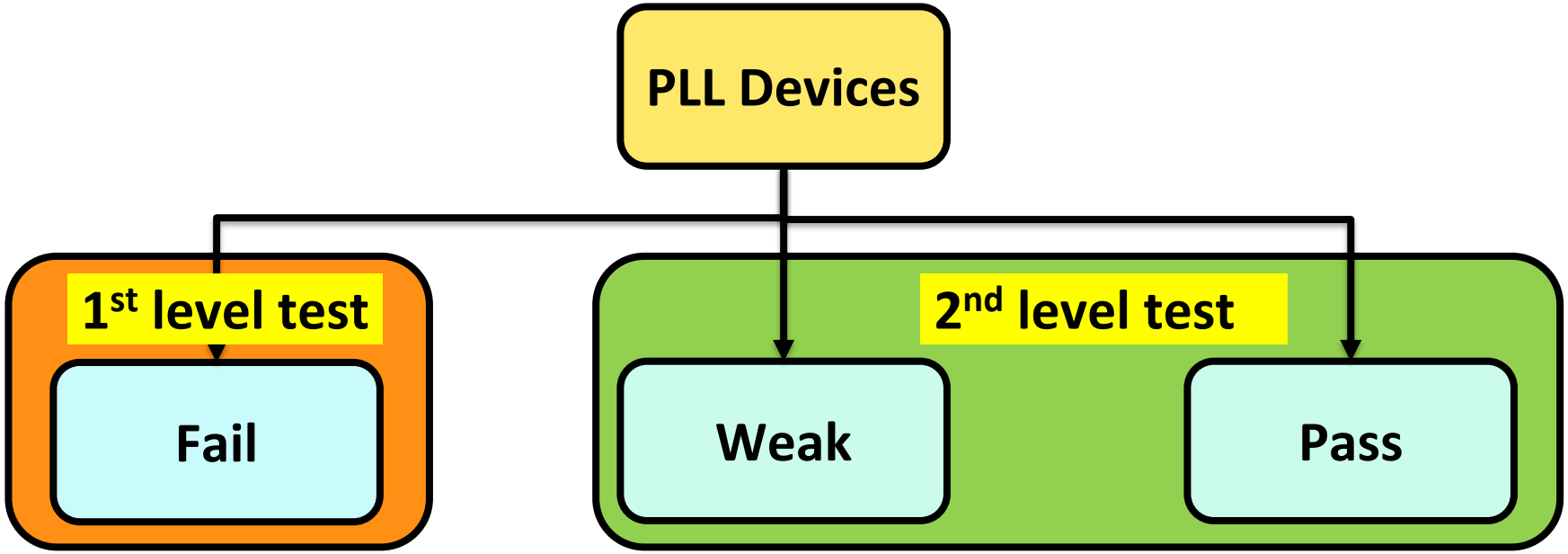
- [min-period, Max period] = [998ps, 1003ps]
- PPJA = 1003-998 = 5ps



Outline

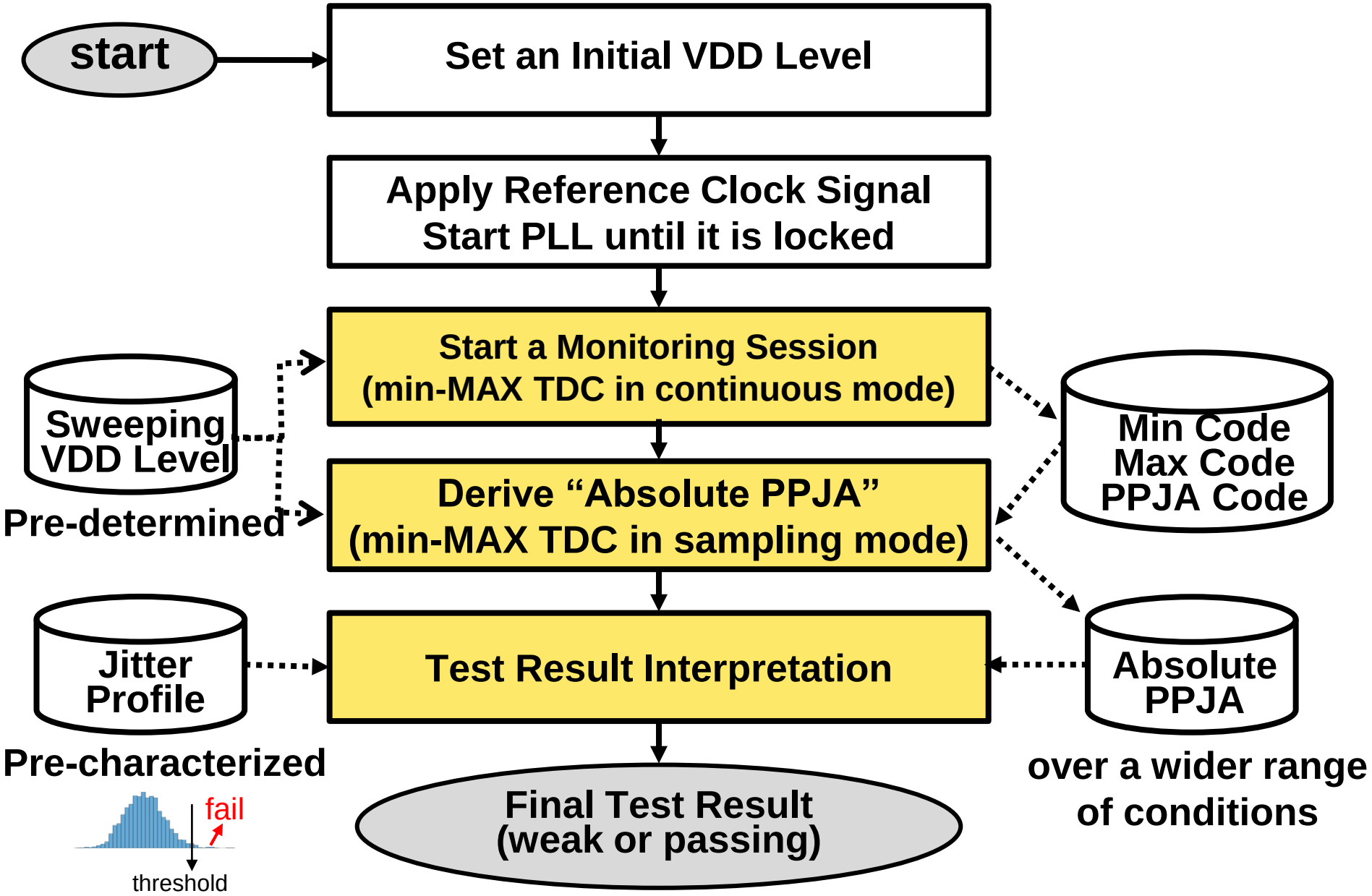
- Introduction
- **Proposed Rigorous Test Flow for PLL using Jitter Measurement**
  - Proposed Jitter Measurement
  - **Proposed Temperature-to-VDD-mapping Scheme**
- Experimental Results
- Conclusion

Classify a PLL Device



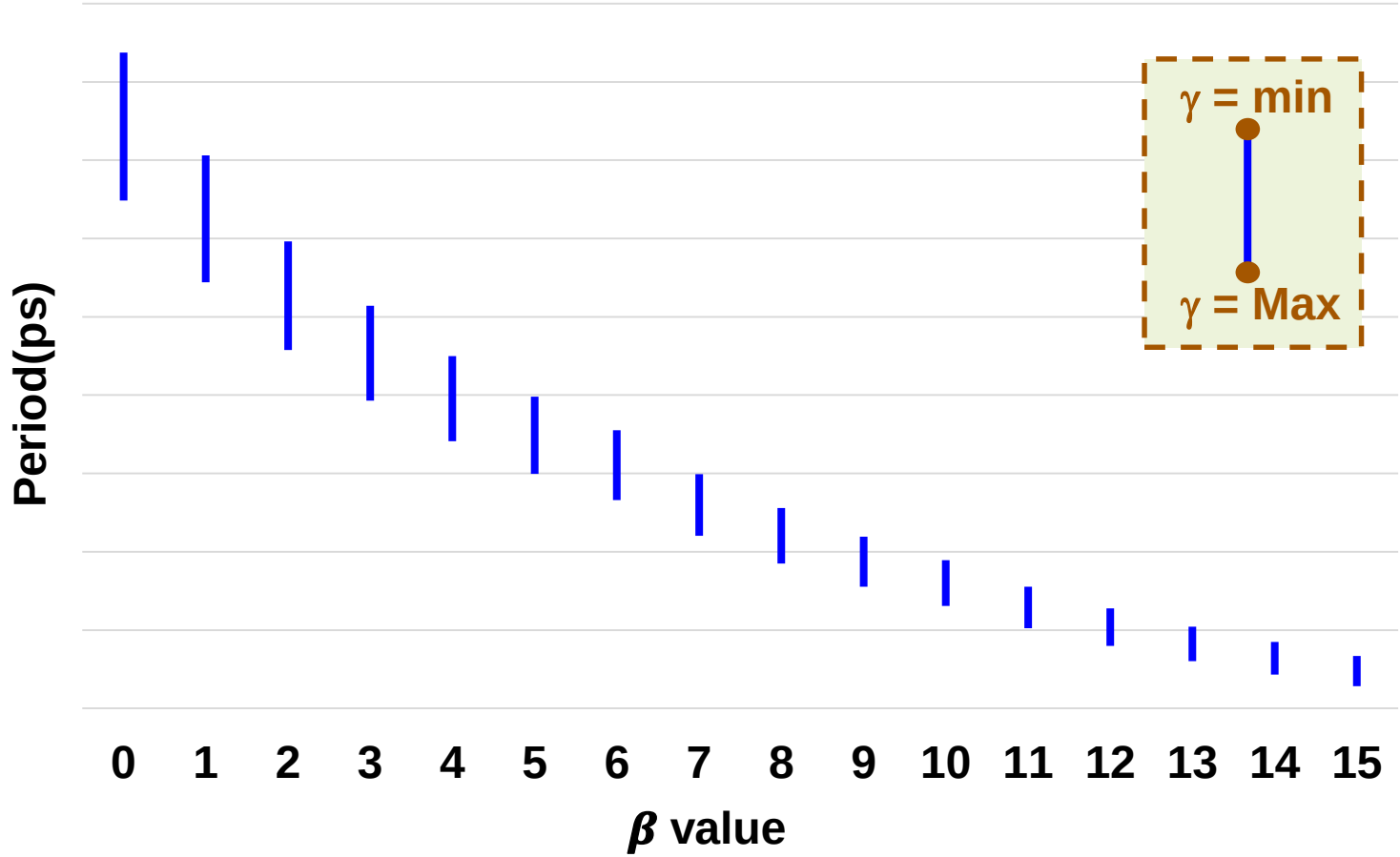
Do not oscillate.
Low frequency accuracy.

Rigorous Test Flow



Temperature-to-VDD-mapping Scheme

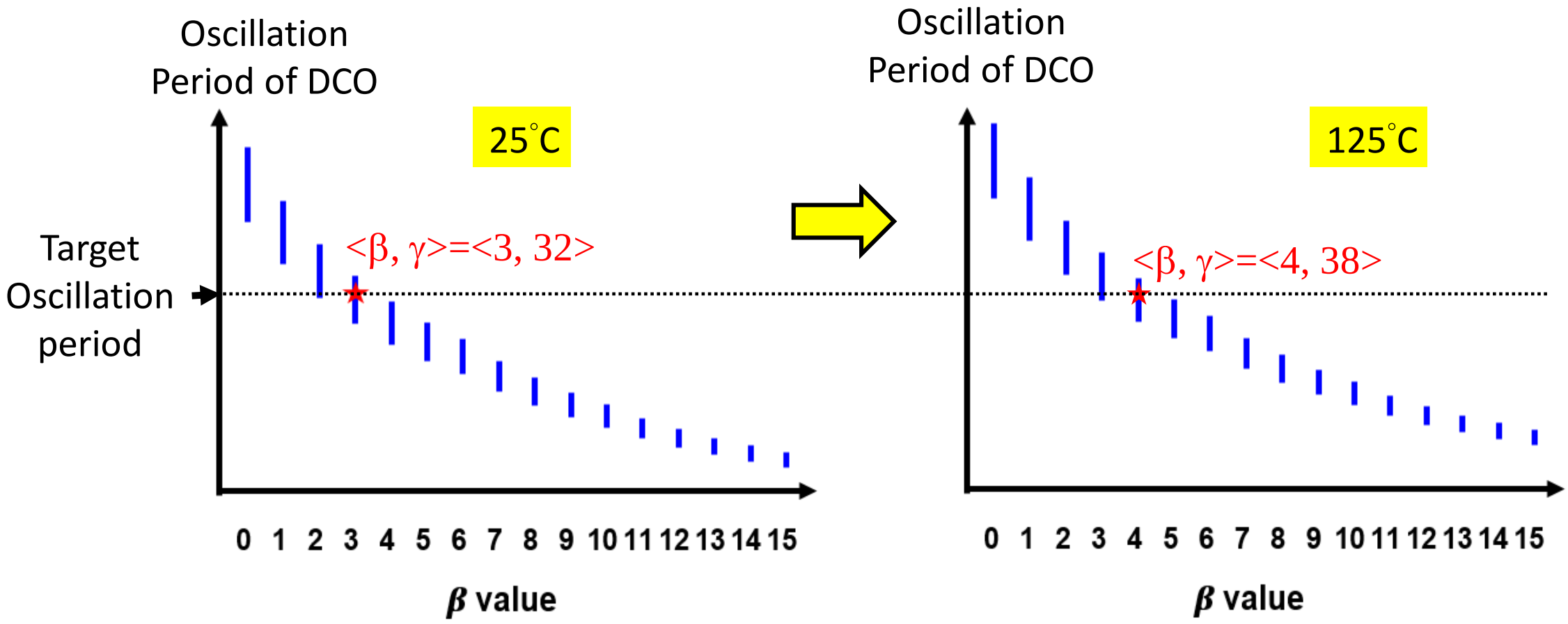
- None of the traditional tests strictly consider the effect of temperature.
- Our DCO is a function of two-level control codes <β, γ>.



Different OP at Different Temperatures

- **Different operating points in the DCO profile at different temperatures.**

OP(VDD, Temperature) = < β, γ >



Different OP at Different Temperatures

OP(VDD, Temperature) = < β, γ >

OP(1V, -40°C) = <2, 49>
OP(1V, 25°C) = <3, 32>
OP(1V, 125°C) = <4, 38>

- **It is much easier to change the VDD level than to change the temperature.**
- **Define a term called "Equivalent VDD level".**

Definition of Temperature-to-VDD-mapping Scheme

- **Equivalent VDD Level for a temperature:**

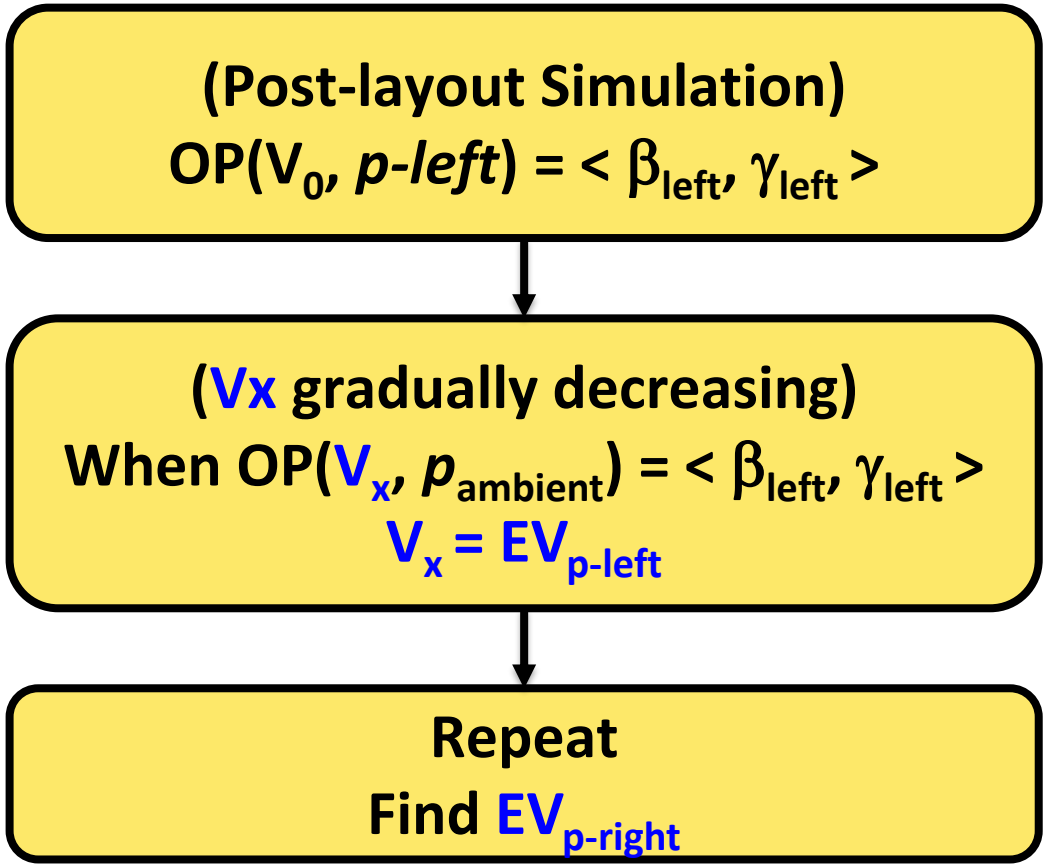
$$OP(V_0, p) = OP(EV_p, p_{amb})$$

$$p = [-40°C, 125°C]$$

- **Notation for Extreme Temperatures:**
  - ***p-left*** **is -40°C and** ***p-right*** **is 125°C.**

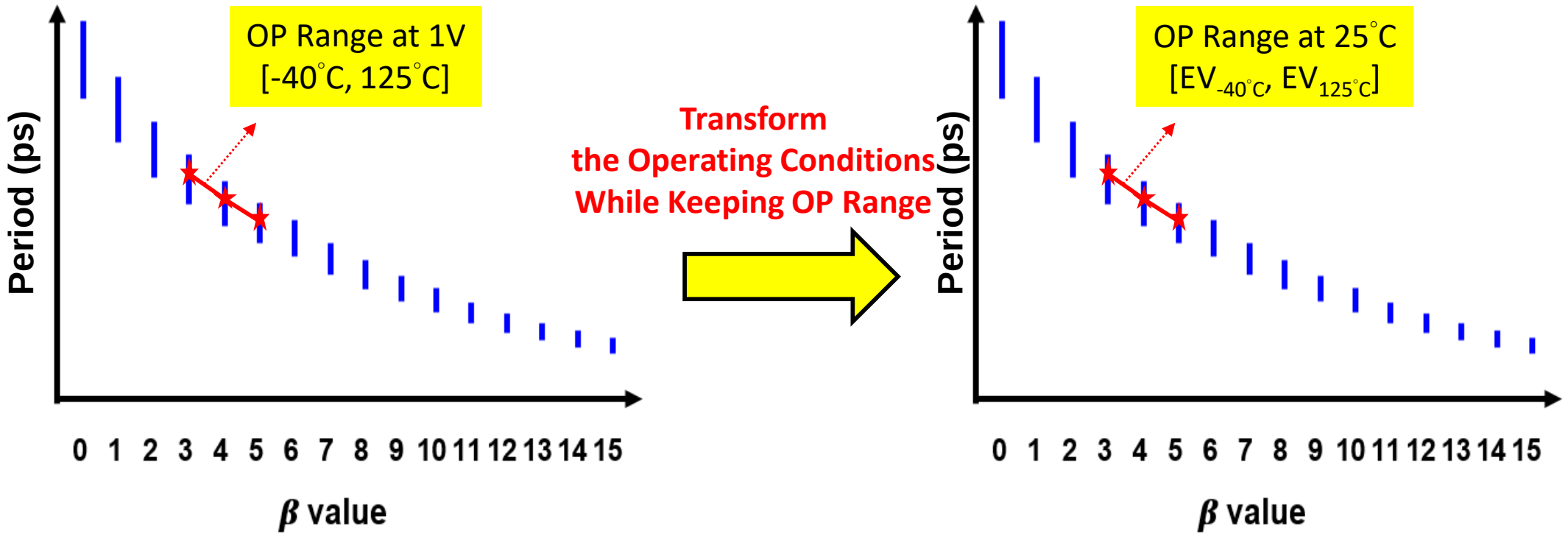
Equivalent VDD level

- To derive the **Equivalent VDD Level** for *p-left* and *p-right*.
  - $EV_{p\text{-}left}$ and $EV_{p\text{-}right}$.
- We use a successive approximation method:



Transforming the Operating Conditions

- **Transforming the operating conditions from [-40°C, 125°C] at 1V to 25°C at [EV-40°C, EV125°C] V, while exercising the same "operating point range"(OP Range) in the DCO profile.**



TDC Resolution Issue

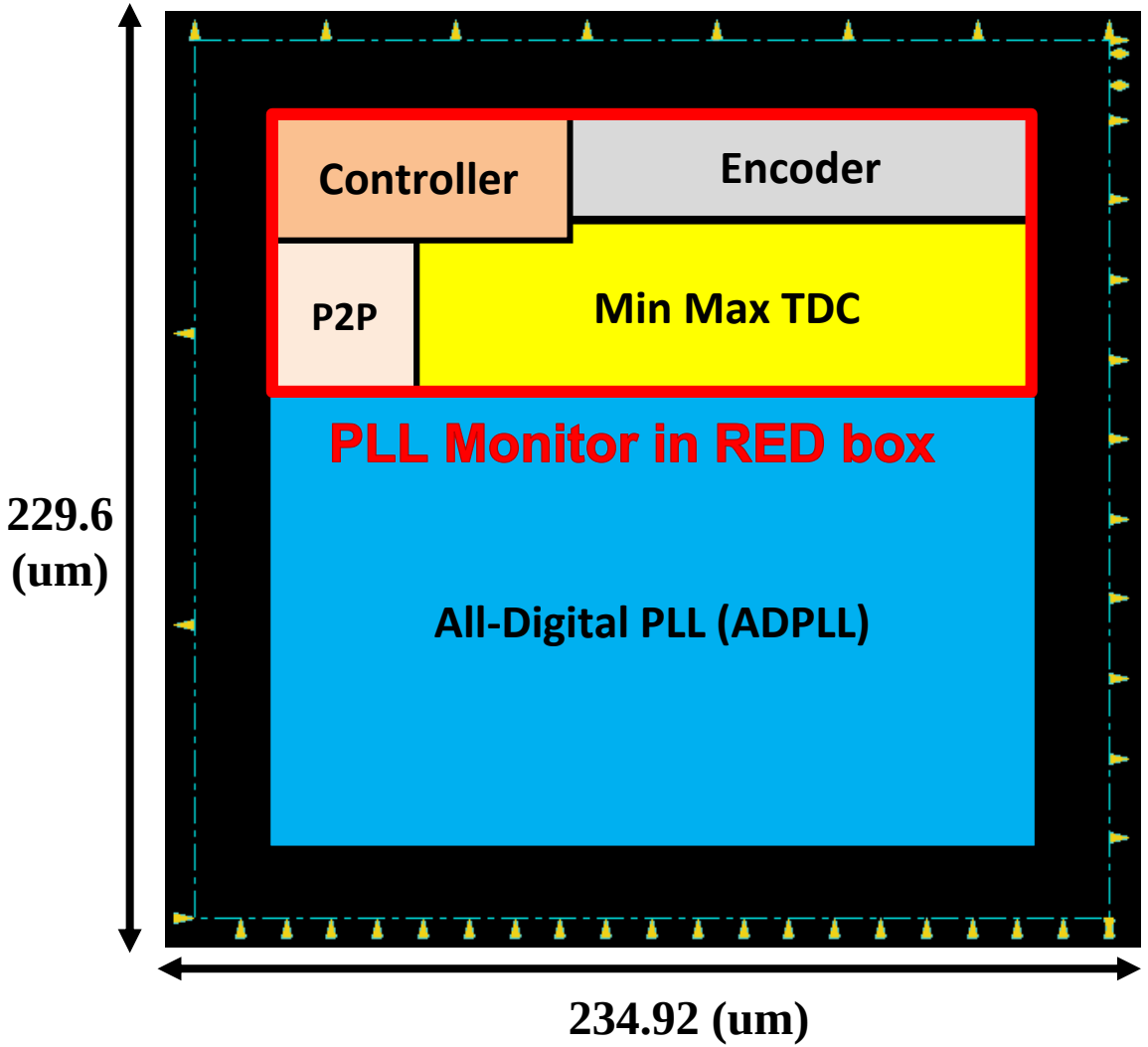
- The code resolution of the TDC is time-varying and affected by VDD level and temperature among other factors.

- Decompose the entire test session into sub-session.
- → Code resolution is constant.

Outline

- Introduction
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- **Experimental Results**
  - Jitter Measurement
  - Temperature-to-VDD-mapping Scheme
- Conclusion

Layout



- Layout in a 90nm CMOS Process
- Power consumption = 4.339 mW.
- The total area is 0.054 mm^2.
  - The area of proposed Monitor is 0.021 mm^2.
  - The area of ADPLL is 0.033 mm^2.

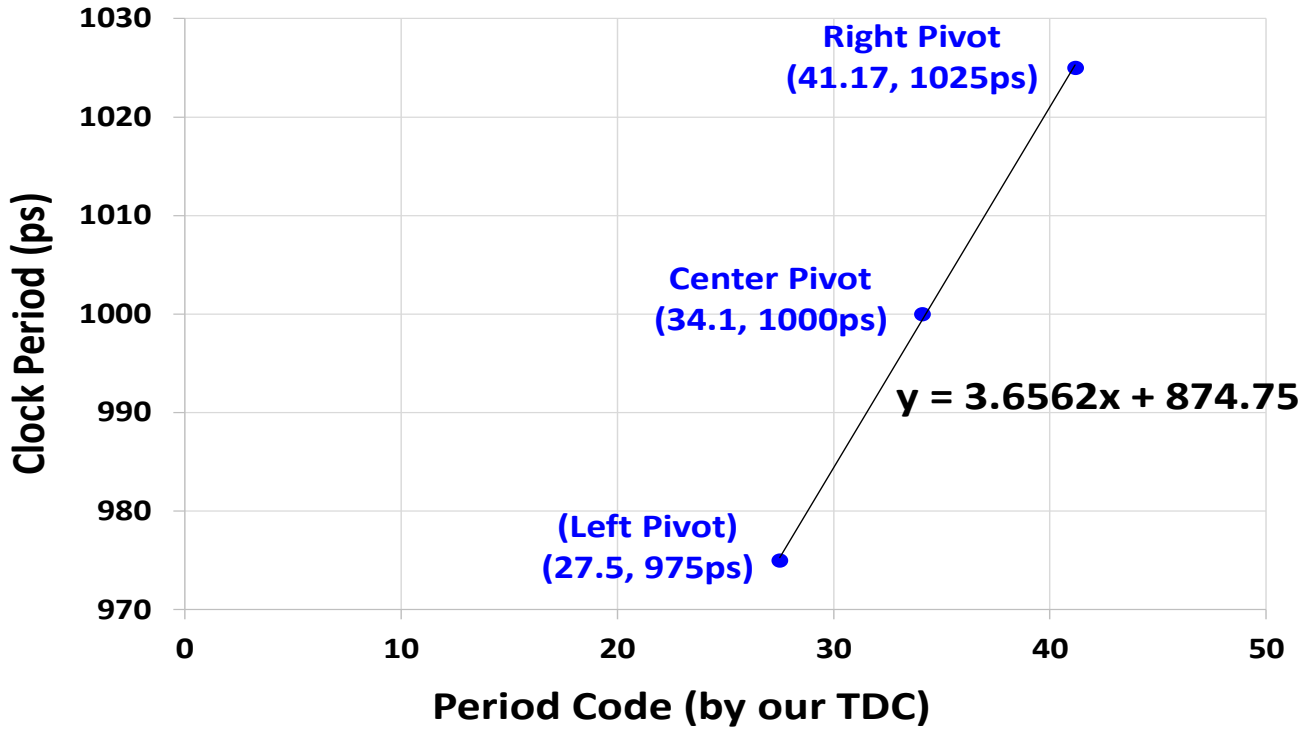
Outline

- Introduction
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- **Experimental Results**
  - **Jitter Measurement**
  - Temperature-to-VDD-mapping Scheme
- Conclusion

Result of 3 pivot points for 1GHz PLL

The 3 pivot points for 1GHz PLL

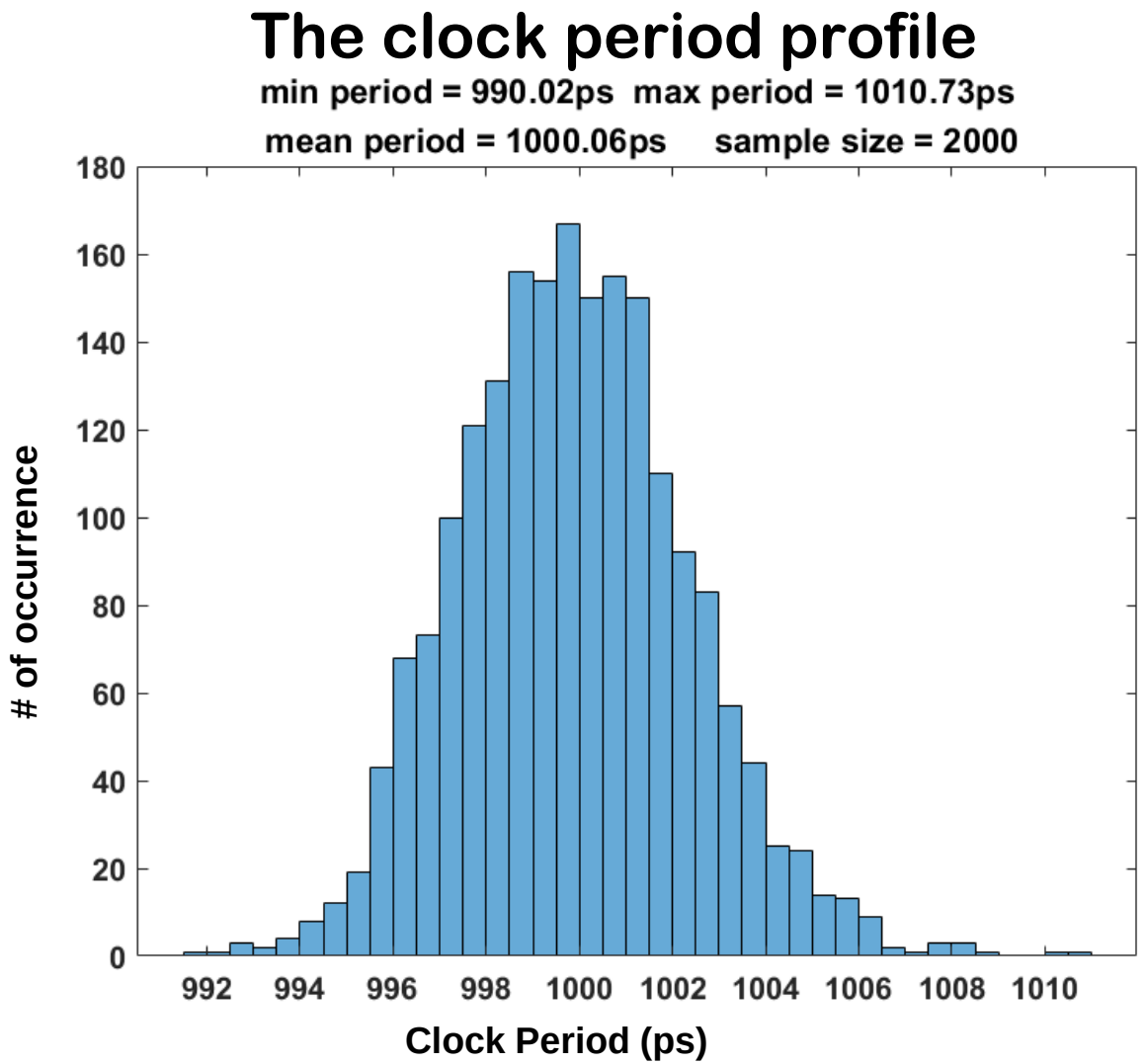
Pivot Points	Dithering Size	Multiplicative Factor (N.f)	Ideal Clock Period	Actual Average of 128 Clock Period Samples	Average of the 128 Period Codes Reported
Center	0	41.67	1000ps	999.97ps	34.1
Left	-25ps	42.73	975ps	975.02ps	27.5
Right	+25ps	40.65	1025ps	1024.95ps	41.17



- **Example:**

1) $Pivot_{center}$= (34.1, 1000ps)
   $Pivot_{right}$= (41.17, 1025ps)
   $Pivot_{left}$= (27.5, 975ps)
2) Linear Transfer Function:
   y=3.6562x+874.75
3) Resolution(LSB) = 3.6562ps
4) [min-code, Max-code] = [31, 38]
   ↓ y=3.6562x+874.75
5) [min-period, Max-period]
   = [991.75, 1013.69]
6) PPJA = 21.94 ps

Result of 3 pivot points for 1GHz PLL



	Dithering-Based	Direct Waveform Analysis	Error (ps)
min-period (ps)	991.75	990.02	1.73
Max period (ps)	1013.69	1010.73	2.96
Peak-to-Peak Jitter (ps)	21.94	20.71	1.23

Result of Jitter Measurement

- Jitter measurement results for 2 ADPLL designs.

Target Frequency (MHz)	Target Clock Period (ps)	Avg. Clock Period (ps)	Peak-to-Peak Jitter (ps)		LSB Resolution of our TDC (ps)	Error* (ps)
			Direct Waveform Analysis	Ours		
1000	1000	1000.06	20.71	21.94	3.6562	1.23
1152	868	868.14	16.5	17.72	3.5433	1.22

* Error < 1LSB

- Due to the simulation time, we only set clock period samples = 128.
- Calibration Time = 110μs when clock period samples = 1024.

Outline

- Introduction
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- **Experimental Results**
  - Jitter Measurement
  - **Temperature-to-VDD-mapping Scheme**
- Conclusion

VDD level sweeping from 0.95V to 1.04V

- OP(1V, -40°C) = <2, 49> = OP(1.04V, 25°C)
- OP(1V, 125°C) = <4, 38> = OP(0.95V, 25°C)

Mapping Temp.

125°C ↑ 25°C ↓ -40°C

Test Session	VDD Level (V)	Avg. PLL's Output Clock Period (ps)	Value of PPJA Code	TDC's Code Resolution (ps)	Peak-to-Peak Jitter (PPJA) (ps)		Error (ps)
					Direct Waveform Analysis (Reference)	Our Method	
1	0.95	1000.032	7	3.53	22.29	24.71	2.42
2	0.96	1000.432	12	3.53	42.00 max	42.36	0.36
3	0.97	999.506	10	3.54	34.59	35.4	0.81
4	0.98	1000.018	9	3.62	30.95	32.58	1.63
5	0.99	1000.745	9	3.64	29.54	32.76	3.22
6	1	1000.117	9	3.66	33.57	32.94	0.63
7	1.01	1000.497	8	3.73	28.12	29.84	1.72
8	1.02	1000.123	10	3.74	37.45	37.4	0.05
9	1.03	1000.124	8	3.75	32.70 min	30	2.7

VDD level sweeping from 0.95V to 1.04V

Test Session	VDD Level (V)	Avg. PLL's Output Clock Period (ps)	Value of PPJA Code	TDC's Code Resolution (ps)	Peak-to-Peak Jitter (PPJA) (ps)		Error (ps)
					Direct Waveform Analysis (Reference)	Our Method	
1	0.95	1000.032	7	3.53	22.29	24.71	2.42
2	0.96	1000.432	12	3.53	42.00	42.36	0.36
			⋮				
6	1	1000.117	9	3.66	33.57	32.94	0.63
10	1.04	999.994	5	3.75	20.40	18.75	1.65

max

min

Reported PPJA range = [18.75ps, 42.36 ps],

Wide-Range PPJA gap = 42.36 – 18.75 = 23.61ps

Nominal Reported PPJA at 1V = 32.94ps

Rigorous Test Gain = 42.36ps – 32.94ps = 9.42ps or (28.6% worse)

Outline

- Introduction
- Proposed Rigorous Test Flow for PLL using Jitter Measurement
- Experimental Results
- **Conclusion**

Conclusion

- Faster clock period monitoring and jitter measurement scheme for a PLL with min-MAX TDC and Dithering-Based Calibration. 10ms → $110\mu s$.

- Support online jitter validation.
- (Map the digital code [min-code, Max-code] into the absolute amounts [min-period, Max-period] in pico-second.)

- Classify PLL device by temperature-to-VDD-mapping scheme to support the transformation of test conditions to make the test easier.
- → not using the support of a thermal chamber.

Thanks for your attention!

Reference

[1] T. H. Kim, R. Persaud, and Chris H. Kim. "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits", IEEE Journal of Solid-State Circuits, Vol. 43, No. 4, pp. 874-880, 2008.

[2] Y. Li, Y. M. Kim, E. Mintarno, D. S. Gardner, and S. Mitra, “Overcoming Early-Life Failure and Aging for Robust Systems,” IEEE Design & Test of Computers, Vol. 26, No. 6, pp. 28-39, 2009.

[3] C. Serafy and A. Srivastava, "Online TSV Health Monitoring and Built-In Self-Repair to Overcome Aging", Proc. of IEEE Int'l Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS), pp. 224-229, 2013.

[4] G.-H. Lian, W.-Y. Chen, and S.-Y. Huang, "Cloud-Based Online Ageing Monitoring for IoT Devices”, IEEE Access, Vol. 7, pp. 135954-135971, 2019.

[5] J. Carretero, X. Vera, P. Chaparro, and J. Abella, “Microarchitectural Online Testing for Failure Detection in Memory Order Buffer”, IEEE Trans. on Computers, Vol. 59, No. 5, pp. 623-637, 2010.

Reference

[6] S.-F. Yang, Z.-Y. Wen, S.-Y. Huang, K.-H. Tsai, and W.-T. Cheng, "Circuit and Methodology for Testing Small Delay Faults in the Clock Network", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 37, No. 10, pp. 2087-2097, 2018.

[7] S.-Y. Huang, M.-T. Tsai, H.-X. Li, Z.-F. Zeng, K.-H. (Hans) Tsai, and W-.T. Cheng, "Non-Intrusive On-Line Transition-Time Binning and Timing Failure Threat Detection for Die-to-Die Interconnects," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 34, No 12, pp. 2039-2048, Dec. 2015.

[8] G.-H. Lian, S.-Y. Huang, and W.-Y. Chen, "Cloud-Based PVT Monitoring System for IoT Devices," Proc. of IEEE Asian Test Symp. (ATS), pp. 76-81, Nov. 2017.

[9] H. Shaheen, G. Boschi, G. Harutyunyan, and Y. Zorian, “Advanced ECC Solution for Automotive SoCs”, Proc. of IEEE Int’l Symp. on On-Line Testing and Robust System Design (IOLTS), pp. 71-73, 2017.

[10] F. Su and P. Goteti, “Improving Analog Functional Safety Using Data-Driven Anomaly Detection”, Proc. of IEEE Int’l Test Conf., Paper 13.3, pp. 1-10. 2018.

Reference

[11] S. Sunter and A. Roy, “On-Chip Digital Jitter Measurement, from Megahertz to Gigahertz,” IEEE Design & Test of Computers, July-Aug., pp. 314-321, 2004.

[12] S. Sunter and A. Roy, “Purely Digital BIST for any PLL or DLL”, Proc. of IEEE European Test Symp., pp. 1-6, 2007.

[13] R. Kinger, S. Narasimhawsamy, and S. Sunter, “Experiences with Parametric BIST for Production Testing PLLs with Picosecond Precision”, Proc. of IEEE Int’l Test Conf., pp. 1-9, 2010.

[14] J.-J. Huang and J.-L. Huang, “An Infrastructure IP for On-Chip Clock Jitter Measurement”, IEEE Int’l Conf. on Computer Design, pp. 1-6, 2004.

[15] P.-Y. Chou and J.-S. Wang, “An All-Digital On-Chip Peak-to-Peak Jitter Measurement Circuit with Automatic Resolution Calibration for high PVT-Variation Resilience”, IEEE Trans. on Circuits and Systems-I: Regular Papers, Vol. 66, No. 7, pp. 2508-2518, July 2019.

[16] J. Yu and F. F. Dai, "On-Chip Jitter Measurement Using Vernier Ring Time-to-Digital Converter," Proc. of Asian Test Symp., pp. 167-170, 2010.

Reference

[17] T. Hashimoto, H. Yamazaki, A. Muramatsu, T. Sato, and A. Inoue, "Time-to-Digital Converter with Vernier Delay Mismatch Compensation for High Resolution On-Die Clock Jitter Measurement," Digest of the Int'l Symp. on VLSI Circuits, pp. 166-167, June 2008.

[18] W. Chu and S.-Y. Huang, "Online Safety Checking for Delay Locked Loops via Embedded Phase Error Monitor", IEEE Trans. on Emerging Topics in Computing, (Early Access Article), 2019.

[19] P. Chen, S.-I. Liu, and J.-S. Wu, "A CMOS Pulse-Shrinking Delay Element for Time Interval Measurement," IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, Sep. 2000.

[20] Y. Liu, U. Vollenbruch, Y. Chen, C. Wicpalek, L. Maurer, Z. Boos, and R. Weigel, "Multi-stage Pulse Shrinking Time-to-Digital Converter for Time Interval Measurements," in Proc. of European Microwave Integrated Circuit Conf. (EuMIC), pp. 267-270, 2007

[21]C.-C. Chen, S.-H. Lin, and C.-S. Hwang, "An Area-Efficient CMOS Time-to-Digital Converter Based on Pulse-Shrinking Scheme," IEEE Transactions on Circuits and Systems-II: Express Briefs, vol. 61, no. 3, Mar. 2014.

Reference

[22]C.-H. Wu, S.-Y. Huang, M. Chern, Y.-F. Chou, and D.-M. Kwai, "A Resilient Cell-Based Architecture for Time-to-Digital Converter", Proc. of IEEE Int'l Symp. on VLSI, pp. 7-12, Bochum, Germany, pp. 7-12, July 2017.

[23]C.-H. Wu, S.-Y. Huang, Y.-F. Chou, and D.-M. Kwai, "Time-to-Digital Converter Compiler for On-Chip Instrumentation", IEEE Design and Test (D&T), Early Access Article, 2020.

[24]W.-H. Chen, C.-C. Hsu, and S.-Y. Huang, "Rapid PLL Monitoring By a Novel min-MAX Time-to-Digital Converter", Proc. of IEEE Int'l Test Conf., (ITC), pp. 1-8, 2020.[25]C.-W. Tzeng, S.-Y. Huang, P.-Y. Chao, and R.-T. Ding, "Parameterized All-Digital PLL Architecture and Its Compiler to Support Easy Process Migration," IEEE Trans. on VLSI Systems (TVLSI), Vol. 22, No. 3, pp. 621-630, March 2014.

[26]C.-E. Lee and S.-Y. Huang, "A Cell-Based Fractional-N Phase-Locked Loop Compiler," Proc. of IEEE Int'l Conf. on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design (SMACD), pp. 273-276, (July 2018).