國立清華大學電機研究所
碩士論文口試

Online Peak-to-Peak Jitter Monitoring for A Phase-Locked Loop
用於鎖相迴路的線上峰值抖動監控方法

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Outline

- Introduction
- Revisit Pulse shrinking Time-to-Digital Converter(TDC)
- Proposed Solution
- Circuit Implementation
- Experimental Results
- Conclusion

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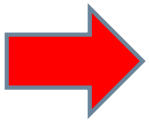
Background

- When the operating speed of the VLSI circuit reaches the GHZ level, the JITTER of the clock signal becomes a key factor affecting the performance of circuit [6].

- In addition, measuring the JITTER of clock signal off chip in pico-second is very costly [4].



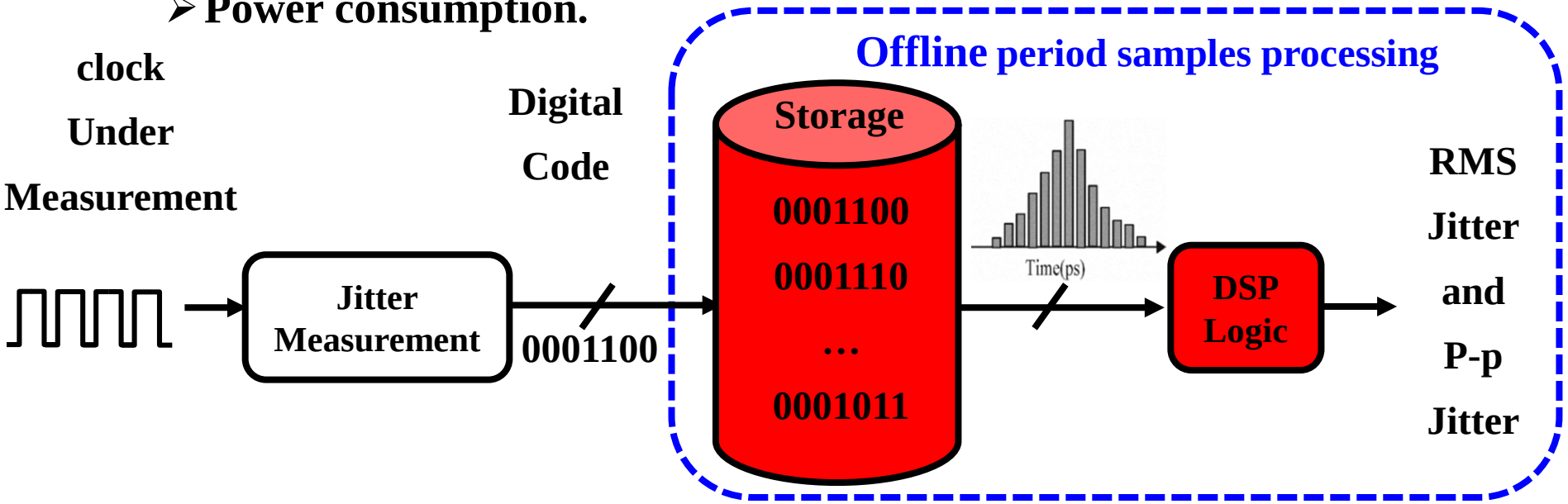
As a result, we require the on chip jitter measurement circuit to ensure the reliability of system.

[4] W. Tang, J. H. Feng, and C. L. Lee, "A Jitter Measurement Circuit Based On Dual Resolution Vernier Oscillator," Proceedings of the IEEE 8th International Conference on Asic, vols 1 and 2, pp. 1213-1216, 2009.

[6] J. Yu and F. F. Dai, "On-chip jitter measurement using vernier ring time-to-digital converter," Asian Test Symposium, pp. 167-170, 2010.

The Conventional Jitter Measurement

- **A large number of off-line jitter samples processing[1].**
  - **Time consumption.**
  - **Power consumption.**

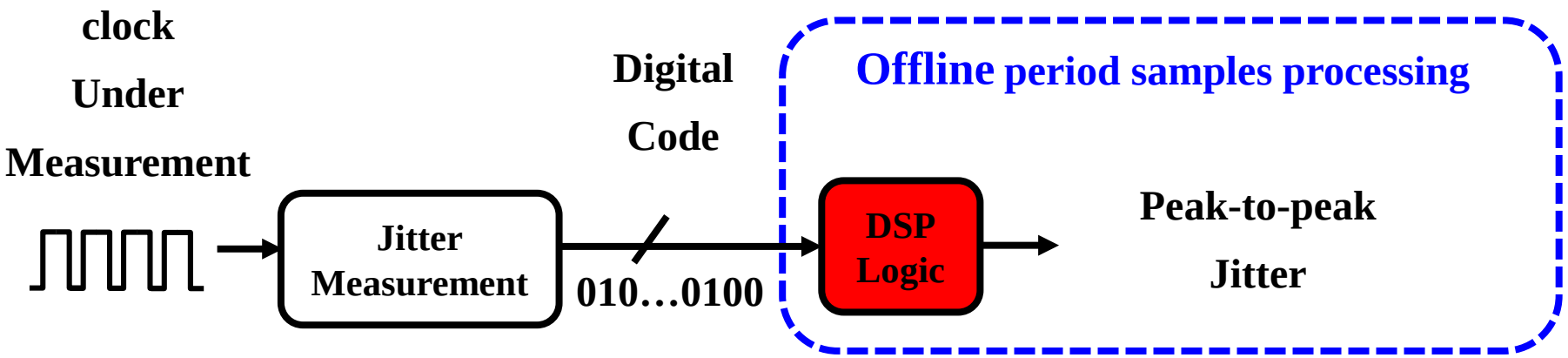


Therefore, we require to reduce the data processing time.

[1] K.A. Jenkins, A.P. Jose and D.F. Heidel, "An on-chip jitter measurement circuit with sub-picosecond resolution", *Proc. Of European Solid-State Circuits Conference (ESSCIRC)*, Vol. 22, No. 3, pp. 157-160, Sept. 2005.

The Recent Jitter Measurement

- 1-time readout peak-to-peak jitter[12].
  - 98% clock cycle reduction and 62% power reduction compared with conventional Jitter measurement.
  - Cannot trace the extreme peak jitter sample in the prior part of measurement session.



Therefore, we propose a solution to trace the extreme peak jitter sample in the whole measurement session.

[12] P.Y. Chou and J.S. Wang, "An All-Digital On-Chip Peak-to-Peak Jitter Measurement Circuit With Automatic Resolution Calibration for High PVT-Variation Resilience", *IEEE Trans. on Circuit and System I: Regular Papers*, pp. 2508-2518, July 2019.

Feature of our jitter measurement

(1) Fully cell based design by using 90nm cell library (easy process migration)

(2) Derive the relative code of peak-to-peak Jitter from the clock under measurement in real time online.

(3) According to transistor-level simulation, the relative code of peak-to-peak Jitter of the clock under measurement is highly correlated to the actual peak-to-peak Jitter value of the clock under measurement .

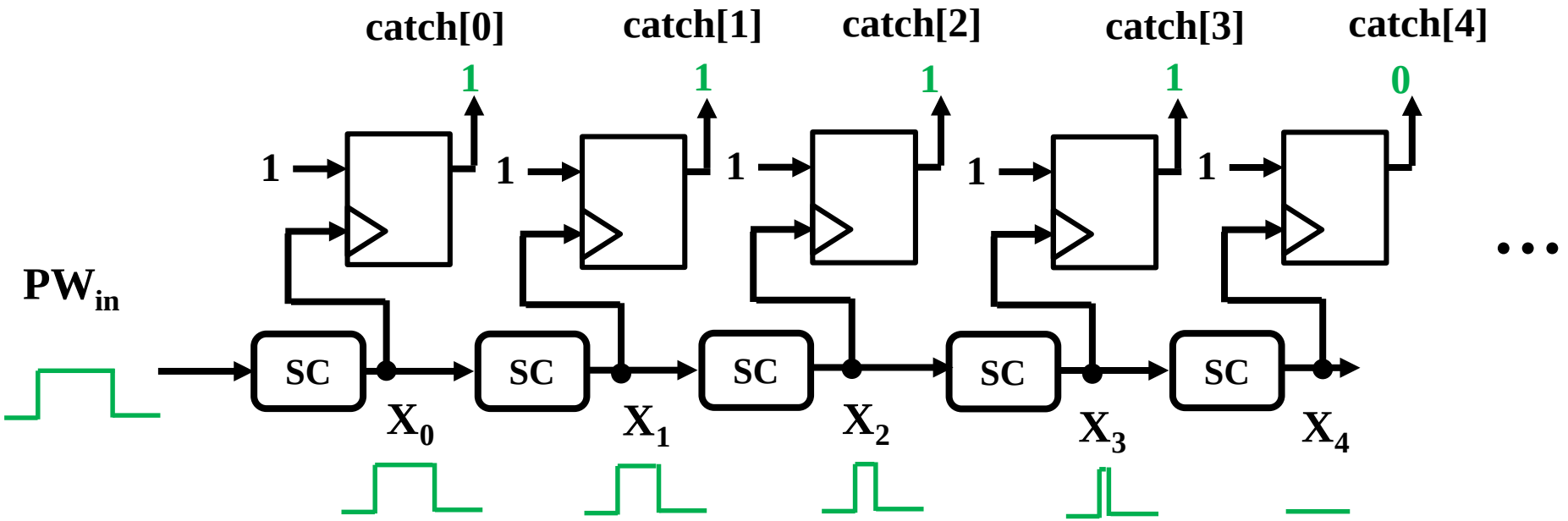
Outline

- Introduction
- **Revisit Pulse Shrinking Time-to-Digital Converter(TDC)**
  - **Operational Principal of Pulse Shrinking TDC**
  - **Restriction of Pulse Shrinking TDC**
- Proposed Solution
- Circuit Implementation
- Experimental Results
- Conclusion

Operational Principal of Pulse shrinking TDC

- pulse shrinking based TDC consists of N stages shrinking cell and N stages D Flip-Flops.[13]

- The incoming pulse will disappear at somewhere in the shrinking line (e.g., X_4.)and produce the output thermometer catch code (i.e., catch[N-1:0]).

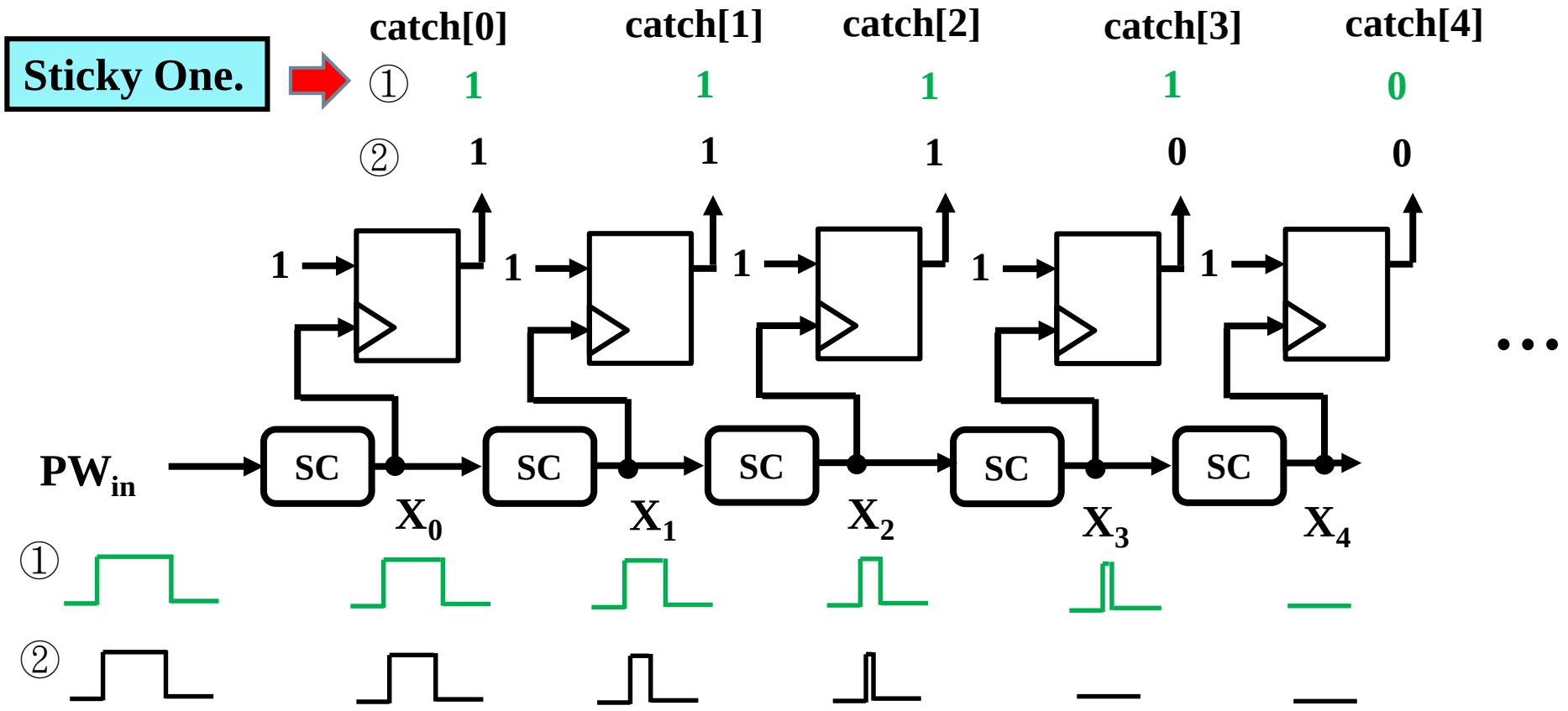


SC means shrinking cell.

[15] C.H. Wu, S.Y. Huang, M. Chern, Y.F. Chou and D.M. Kwai, "Resilient Cell-Based Architecture for Time-to-Digital Converter", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 7–12, July 2017.

Restriction of Pulse Shrinking TDC

- If we send two or multiple pulses into the TDC continuously, we will **only get the thermometer catch code produced by the maximum pulse width** and the pulse width information of other pulse will be covered.[13]



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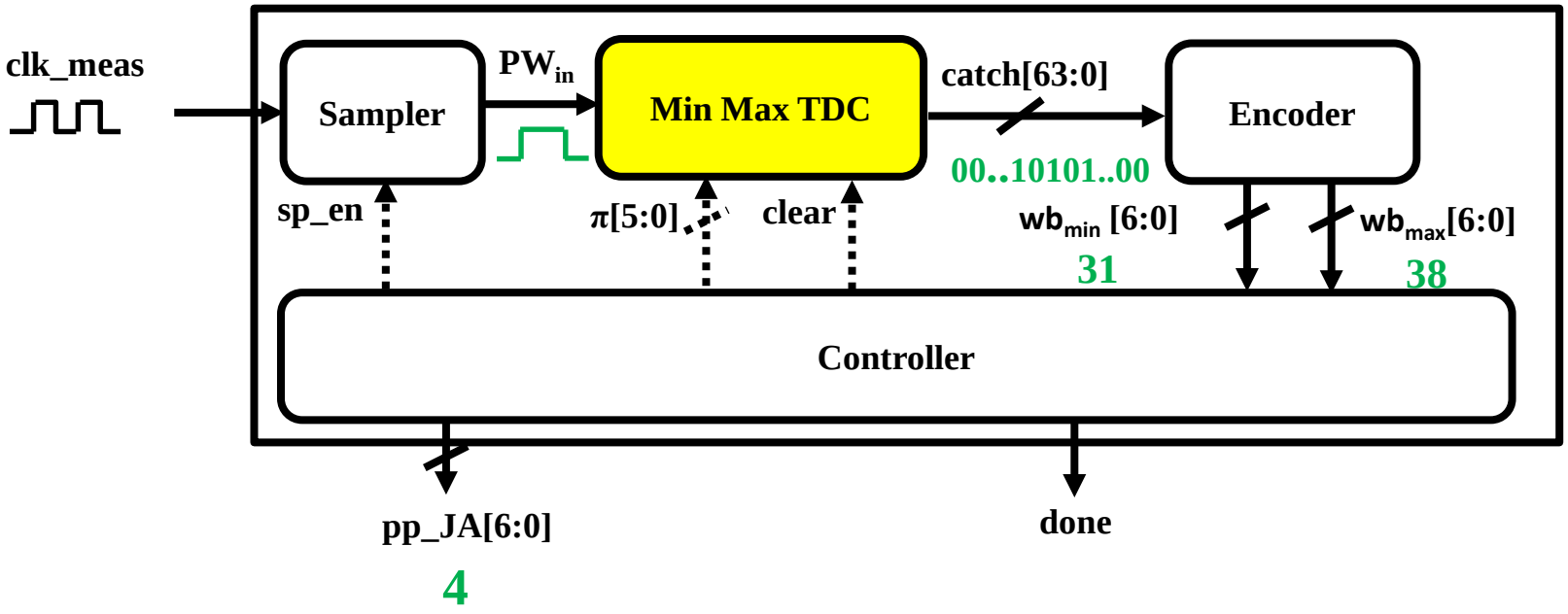
Outline

- Introduction
- Revisit Pulse shrinking Time-to-Digital Converter(TDC)
- **Proposed Solution**
  - **Architecture of Proposed Jitter measurement**
  - **Overall Procedure**
- Circuit Implementation
- Experimental Results
- Conclusion

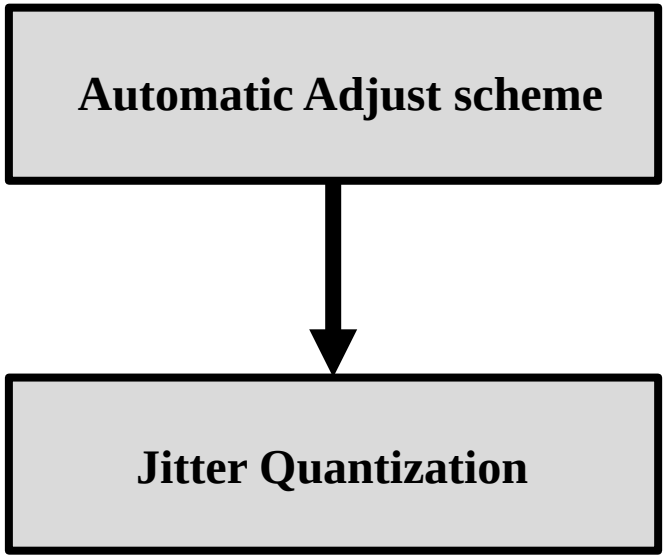
Architecture of Jitter Measurement

- Jitter Measurement(JM) circuit consists of Sampler, Multi-mode Divider, min max TDC, Encoder and Controller.

- JM circuit is used to **measure the peak-to-peak jitter of clock under measurement in a specified time interval.**



Overall Procedure



- Reconfigure the Min Max TDC for **accommodating PVT variation.** (e.g., tune π code .) **[15]**
- Record all incoming period samples by Min Max TDC and finally **report a relative code which implies the peak-to-peak jitter information** among the incoming period samples.

[15] C.H. Wu, S.Y. Huang, M. Chern, Y.F. Chou and D.M. Kwai, "Resilient Cell-Based Architecture for Time-to-Digital Converter", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 7–12, July 2017.

Outline

- Introduction
- Revisit Pulse shrinking Time-to-Digital Converter(TDC)
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- **Circuit Implementation**
  - **Sampler**
  - **Min Max TDC**
  - **Encoder**
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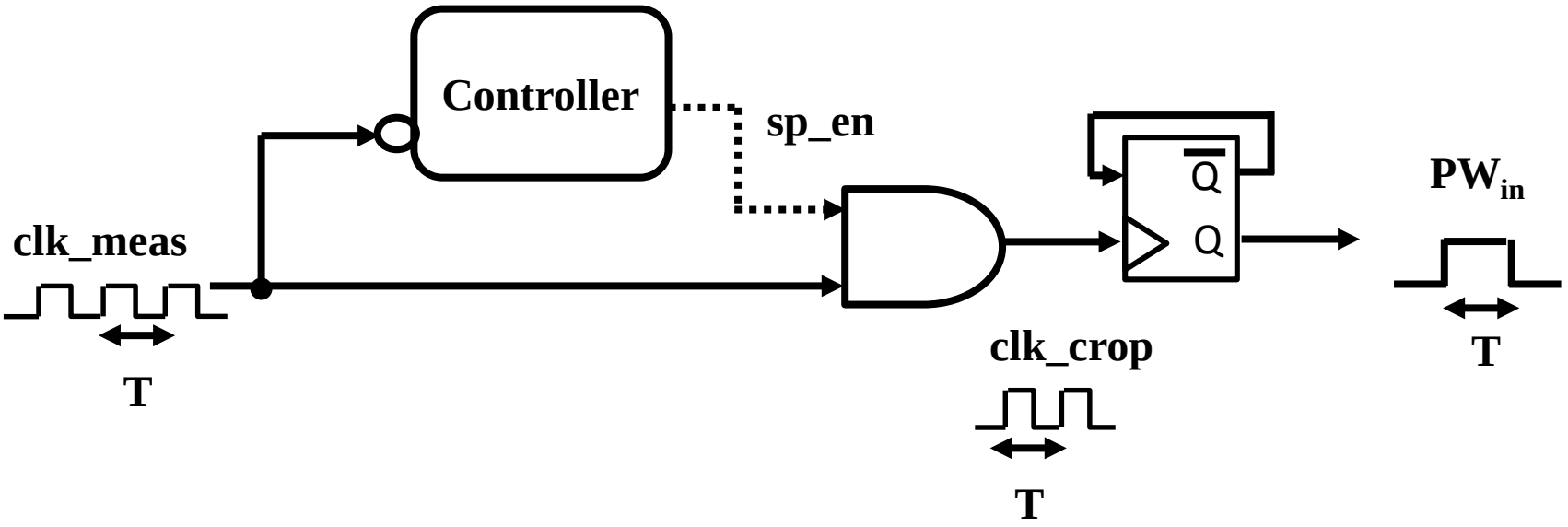
Microarchitecture of Sampler

- **Sampler consists of one 2-input and gate, negative edge-triggered micro-controller and one D-type Flip-flop for monitoring the period information of clock under measurement in a specified time interval.**

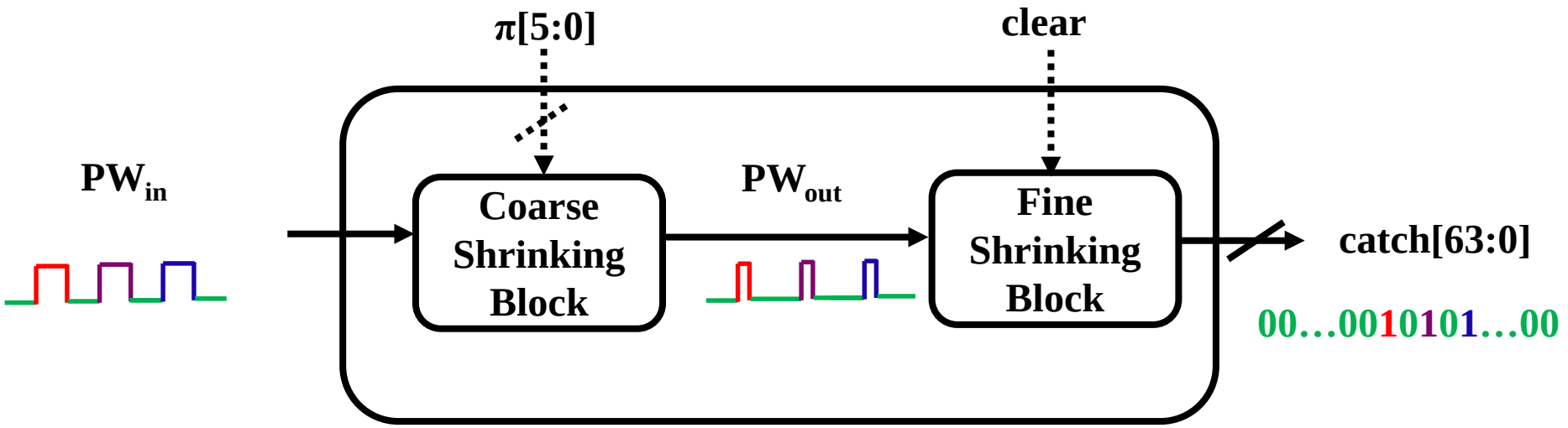
- **Sampler is used to convert the period information into pulse width for the quantization of pulse shrinking-based TDC.**



Microarchitecture of Min Max TDC

- The proposed Min Max TDC consists of coarse shrinking block and fine shrinking block **for record the information all incoming period samples which implies the peak-to-peak jitter information**.

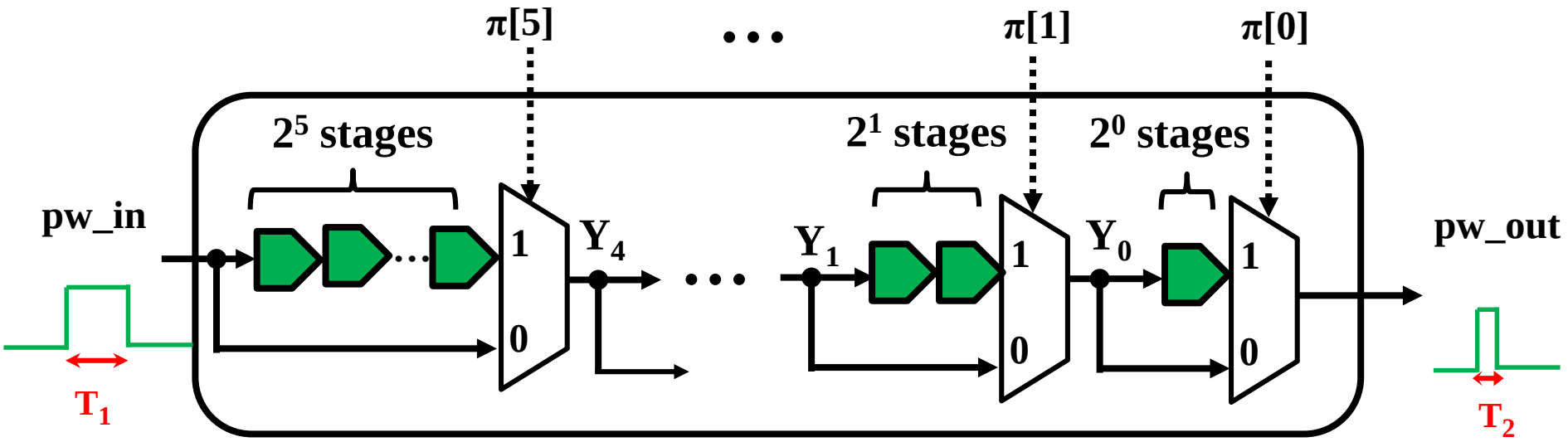
- The proposed Min Max TDC is used to converts the period sample into relative catch bit according to the period rather than thermometer catch code produced by conventional pulse shrinking-based TDC.



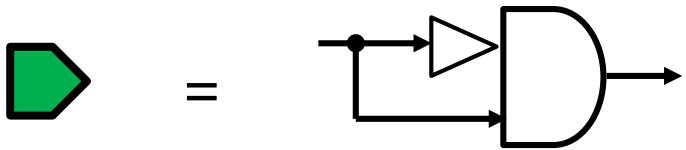
Microarchitecture of coarse shrinking Block

- Coarse shrinking block consists of 63 coarse shrinking cells (CSC) and 6 muxes for accommodating PVT variation.[15]

- Coarse shrinking block is used to significantly shrink the pulse width (e.g., T1.) of incoming pulse to smaller pulse width on output port (e.g., T2.). The π code is used to control the pulse shrinking amount of coarse shrinking block.



CSC = clkbufx1 * 1 + and2x2 * 1

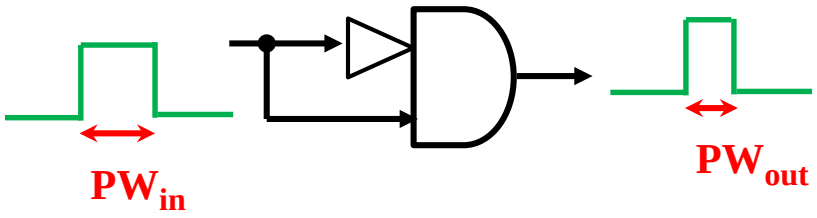


Characteristic of Coarse Shrinking Cell

- **Coarse shrinking cell consists of one clkbufx1 and one and2x2 which are selected from the cell library of 90nm technology. The x1 and x2 means the driving capability of the cell.[15]**

- **The pulse shrinking amount(PSA) from the input of CSC (i.e., *in.*)to the output of CSC (i.e., *out.*) is PW_{in}-PW_{out}.**

clkbufx1 +and2x2

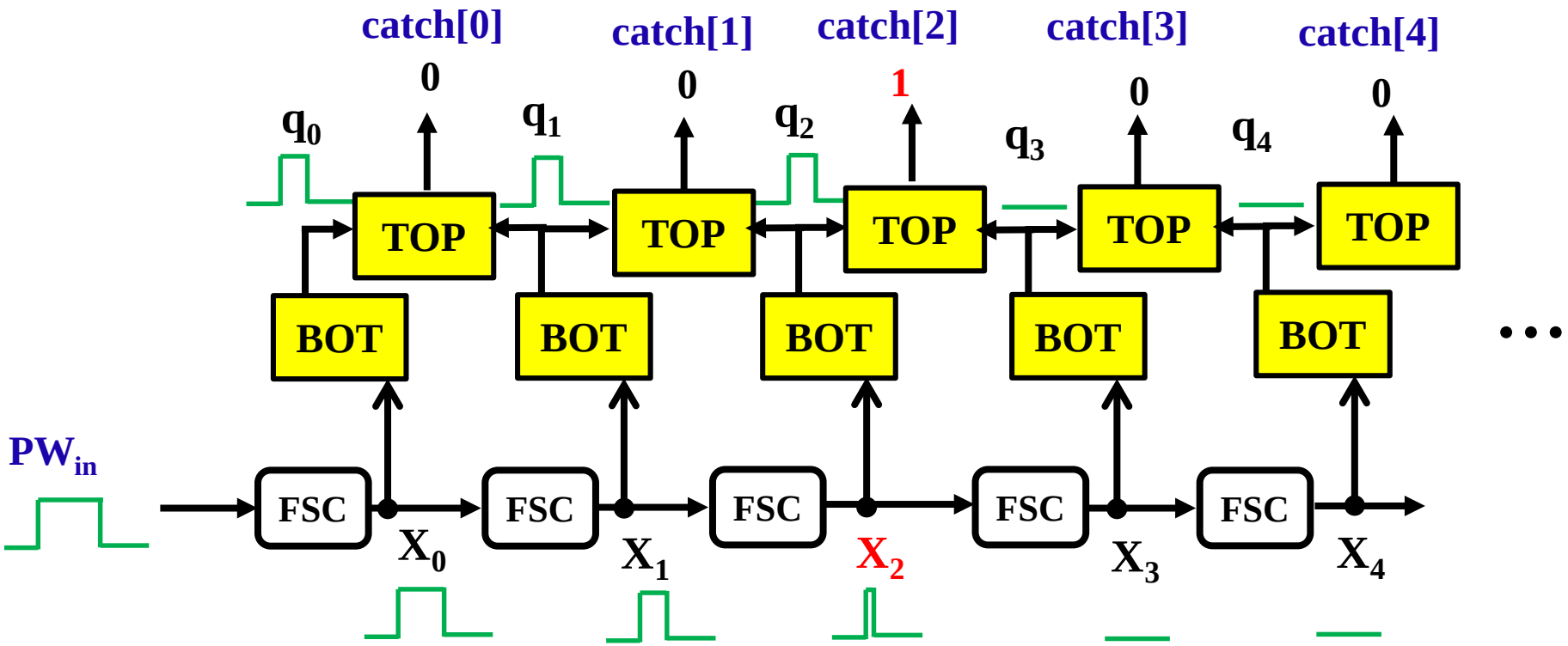


Process corner	SS	TT	FF	SF	FS
PSA (ps)	28.4	22.9	18.8	26.8	19.9

Microarchitecture of Fine Shrinking Block

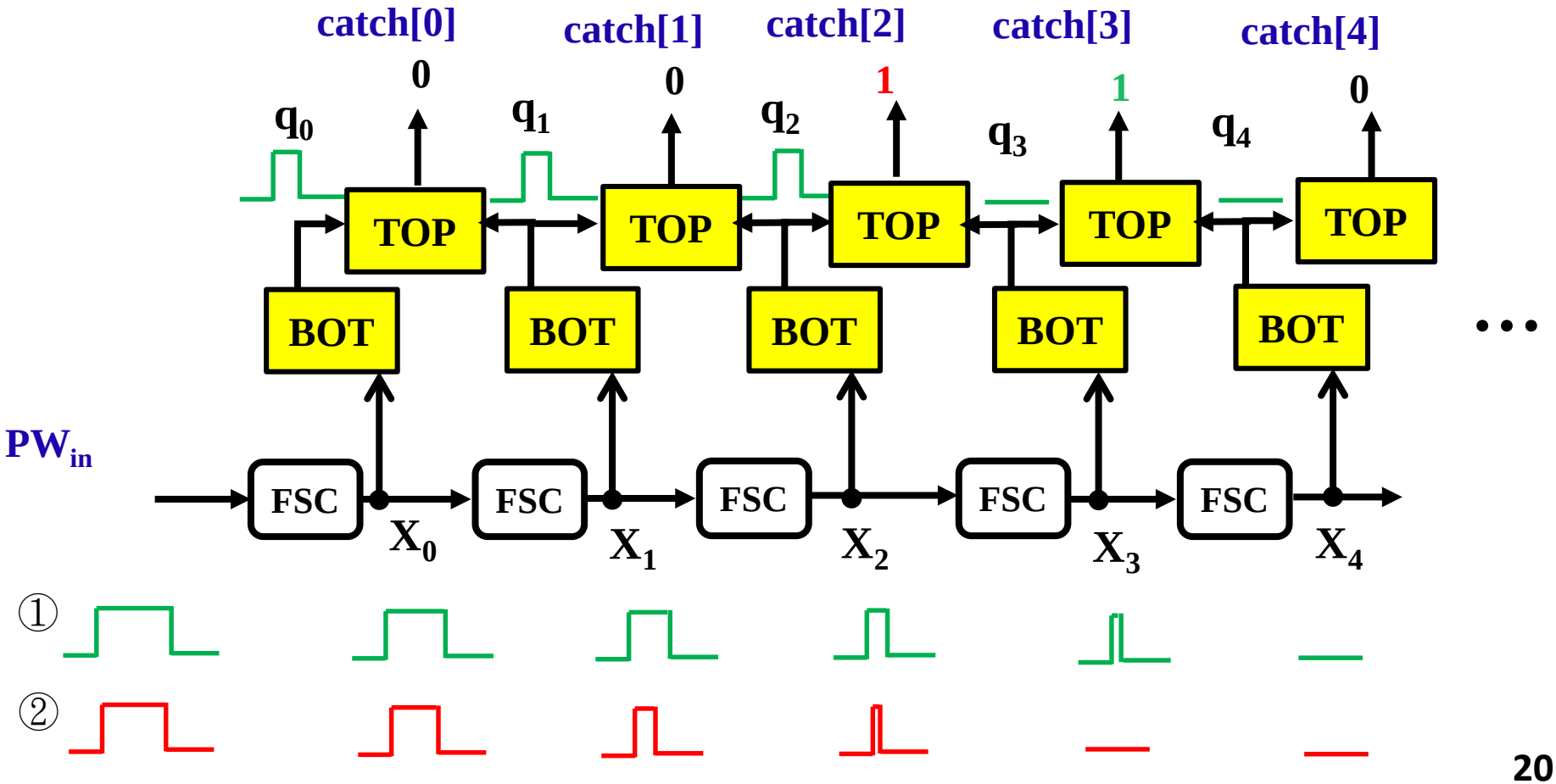
- Fine shrinking block consists of 64 TOP cell, 64 Bottom cell and 64 fine shrinking cell(FSC) for quantizing all incoming period samples.

- The proposed Fine shrinking block is used to convert period sample into relative catch bit according to the period amount. The area of proposed Fine shrinking block is 2.5 times that of conventional fine shrinking block.



Operational Principal of Fine Shrinking Block

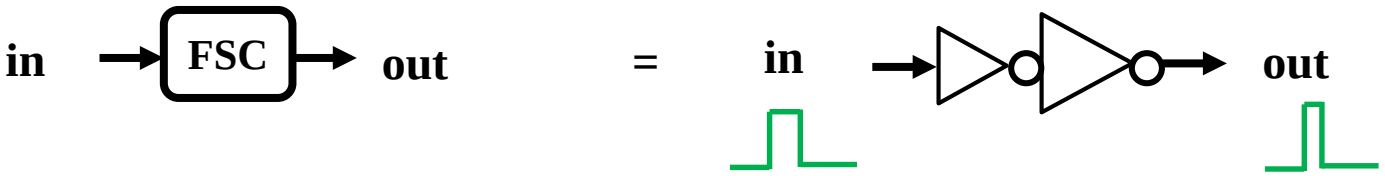
- If we send two or multiple pulses into the PROPOSED TDC continuously, we will get the different catch bit due to the different period samples.
- That means we can quantize all incoming period samples.



Characteristic of Fine Shrinking Cell

- Fine shrinking cell consists of invx1 and invx4 for deciding the resolution of proposed TDC.

- The pulse shrinking amount of fine shrinking cell (e.g., 3.6ps under TT corner.) is as the following table.



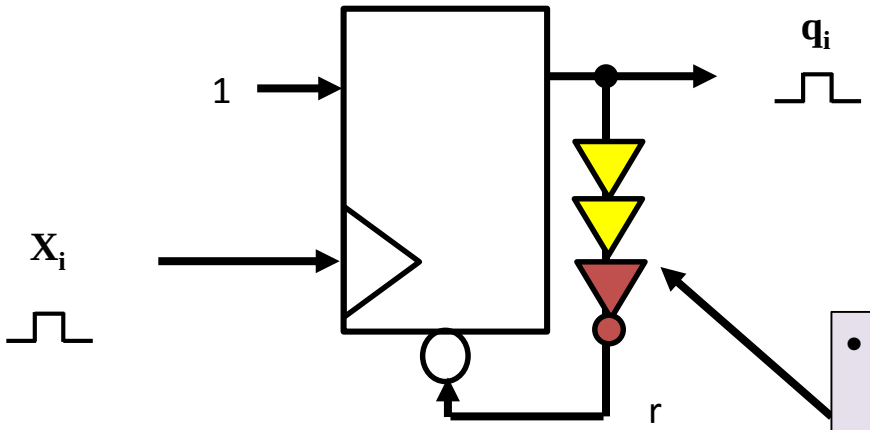
Process corner	SS	TT	FF	SF	FS
PSA (ps)	4.82	3.60	3.06	5.42	1.83

FSC means fine shrinking cell.

Characteristic of Bottom Cell

- Use to produce flag at ***q pin*** for enabling the TOP CELL.
  - If the incoming period sample is alive at X_i.
  - Otherwise, stay zero state at *q pin*.

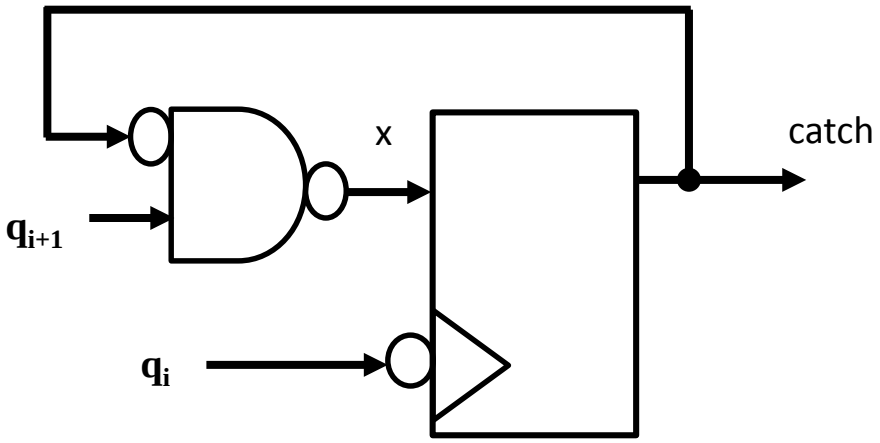
- The pulse width at $\mathbf{q_i}$ pin is about 210ps under typical case.



- **According to our experience, in order to ensure sufficient margin in TOP CELL, we insert two buffer and one inverter here.**

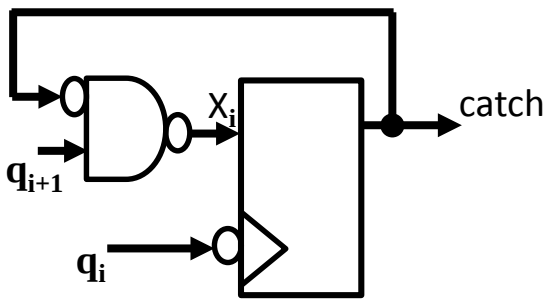
Characteristic of Top Cell

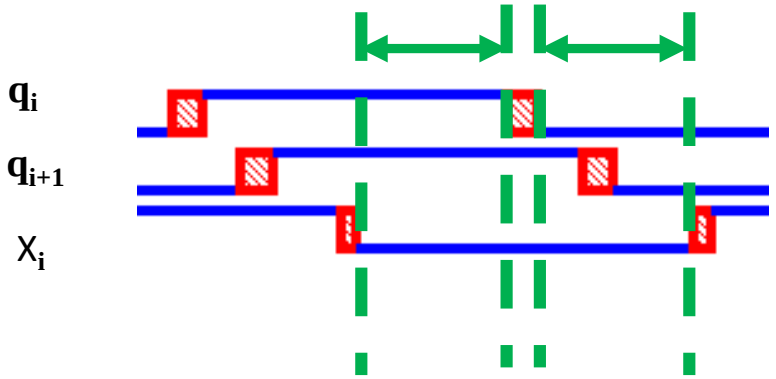
- Use to quantize all incoming period samples continuously.
  - If the catch is zero and q pin has one pulse.
    - If **q_{i+1} has one pulse, the state of catch pin stays zero .**
    - Otherwise, **the state of catch pin changes to one.**
  - Otherwise, stay the state at catch *pin*.



Characteristic of Fine Shrinking Cell

The margin of checking window under 5 corner





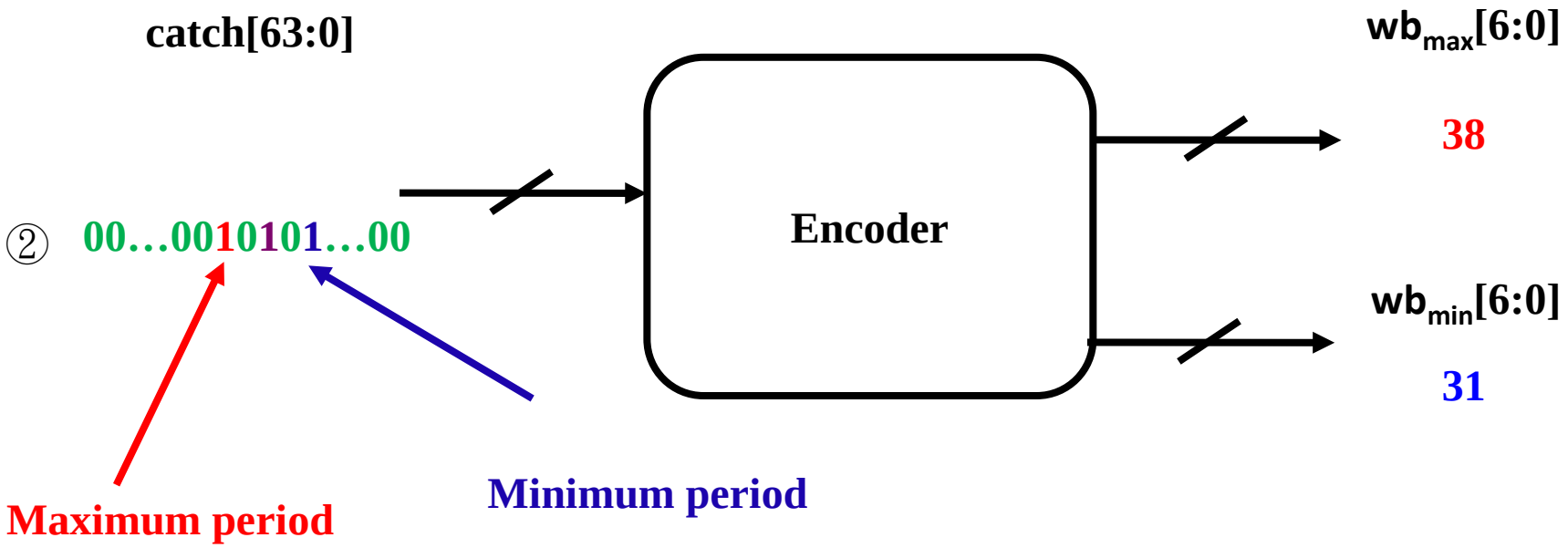
Voltage	1V				
PROCESS	SS	TT	FF	SF	FS
Left margin (ps)	123.59	93.94	74.02	90.98	99.11
Right margin(ps)	124.52	99.68	81.57	98.93	100.21

- The watermark checking cell of **min max TDC** can work correctly.
  - **The minimum left margin is 74ps and minimum right margin is 81ps under process variation.**
  - The area overhead is the 2.5x area of **previous TDC**.

concept of encoder

- Encoder is used to convert the index of catch bit into binary wb_{min} (and wb_{max}) which represents the minimum(and maximum) period information among the incoming period samples.

- Use two if-else block to implement the encoder and the propagation delay of longest path is 2 ns in 90nm technology.



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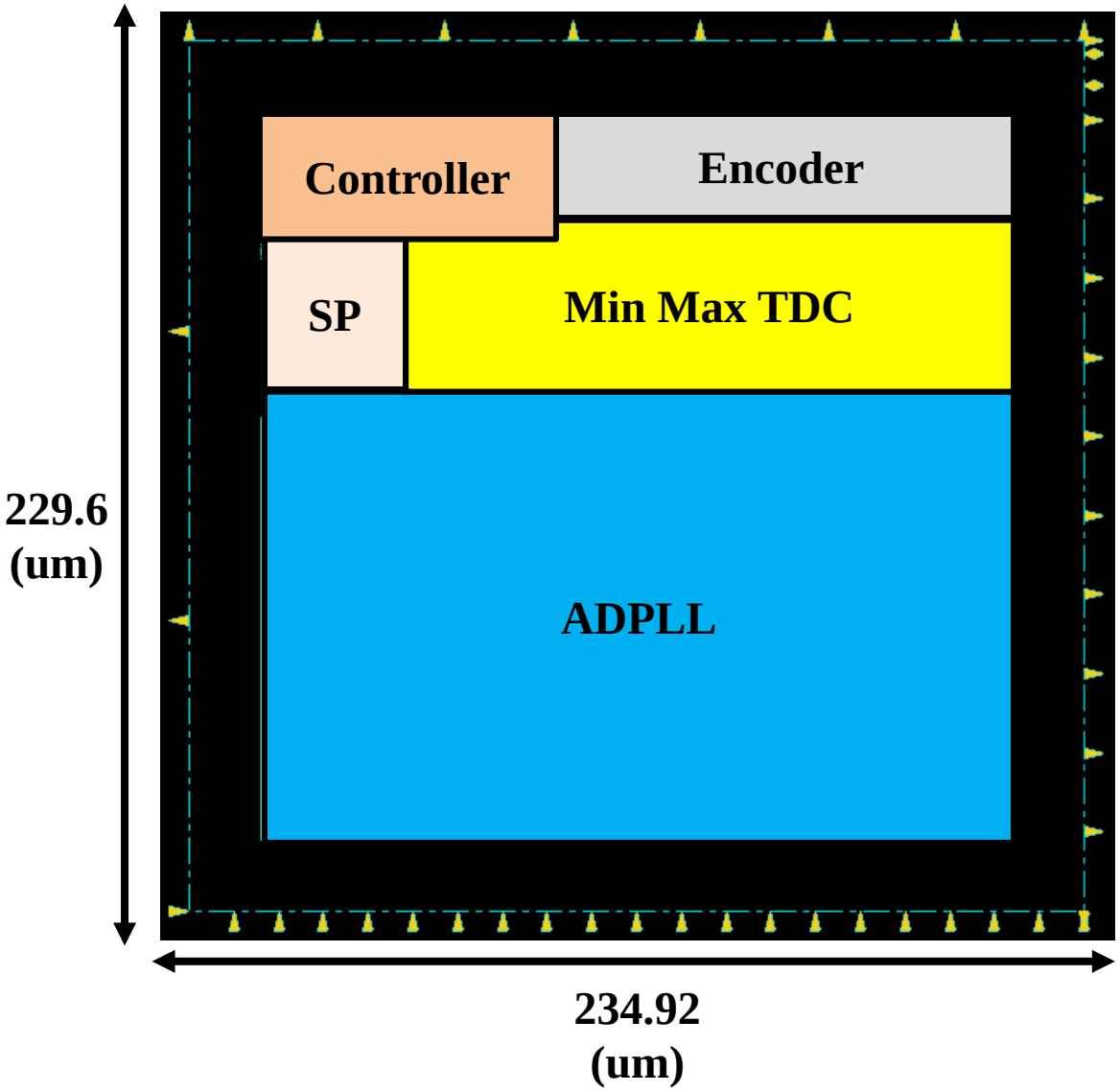
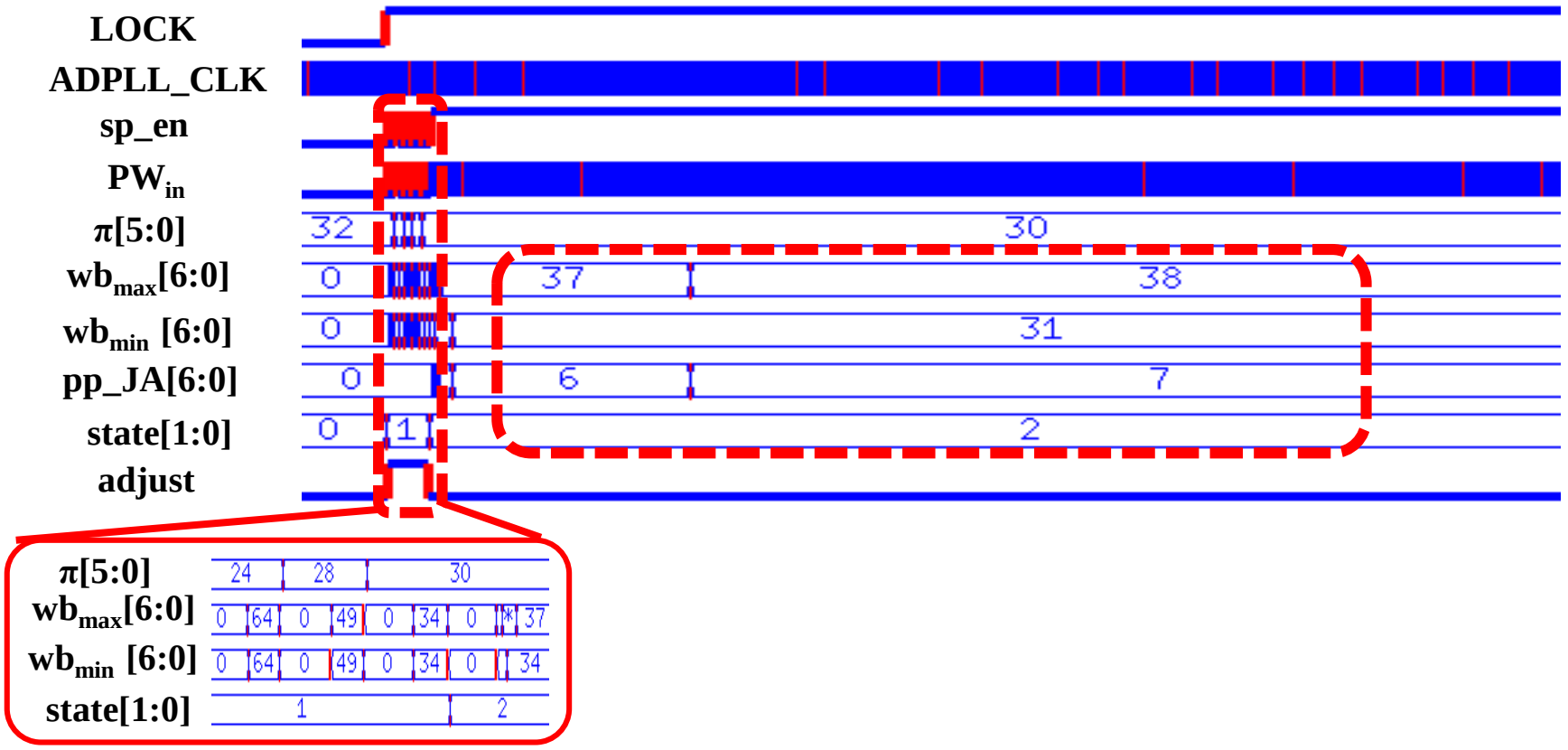
- **Experimental Results**
  - **Layout**
  - **Functional Waveform**
  - **Performance Compared Table**
- Conclusion

The physical Layout of Jitter Measurement



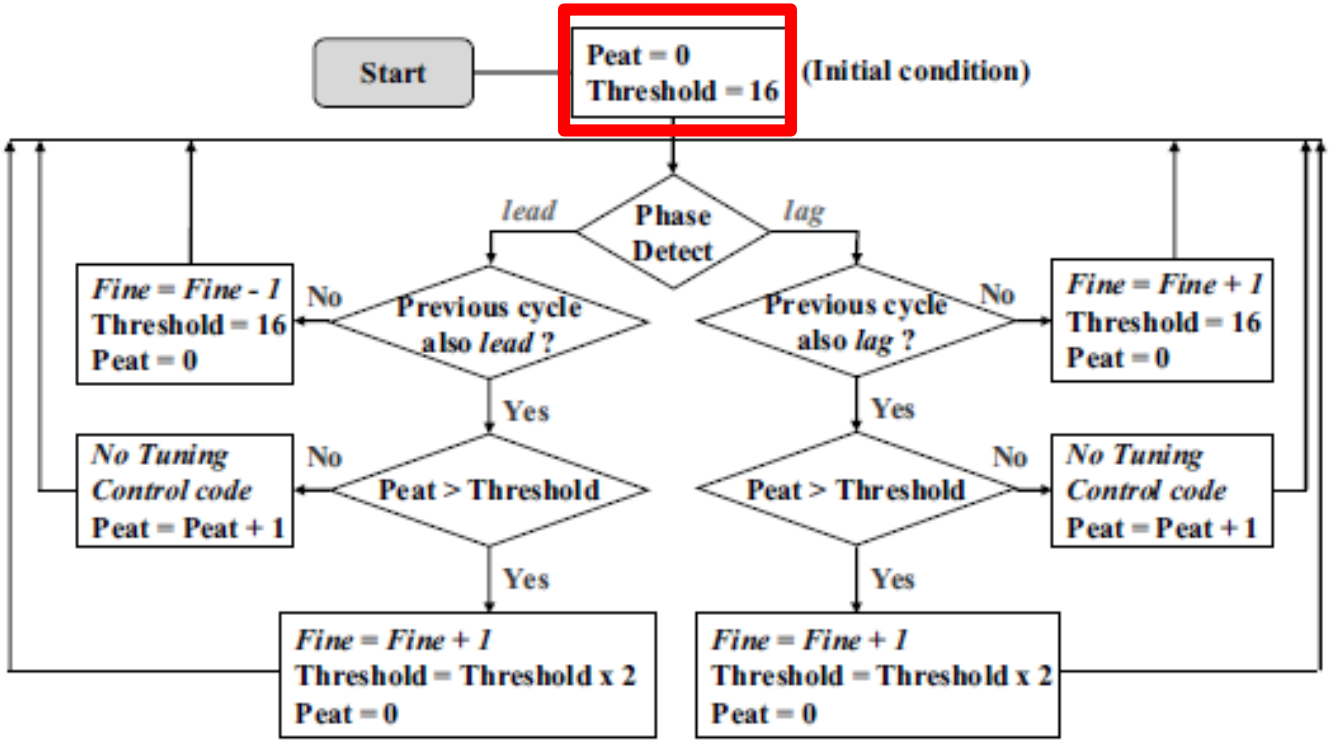
- The physical layout of whole system uses **90nm technology**.
- The total area is 0.054 mm^2.
- **The area of proposed jitter measurement is 63.6% of that of ADPLL.**
  - ✓ The area of proposed Jitter measurement is 0.014 mm^2.
  - ✓ The area of ADPLL is 0.022 mm^2.

Waveform under Typical Case



The initial window size of ADPLL

- In order to verify our Jitter measurement, we try to change the initial window size(or called threshold.) of our ADPLL [11][14] and measure the peak-to-peak jitter of output clock.

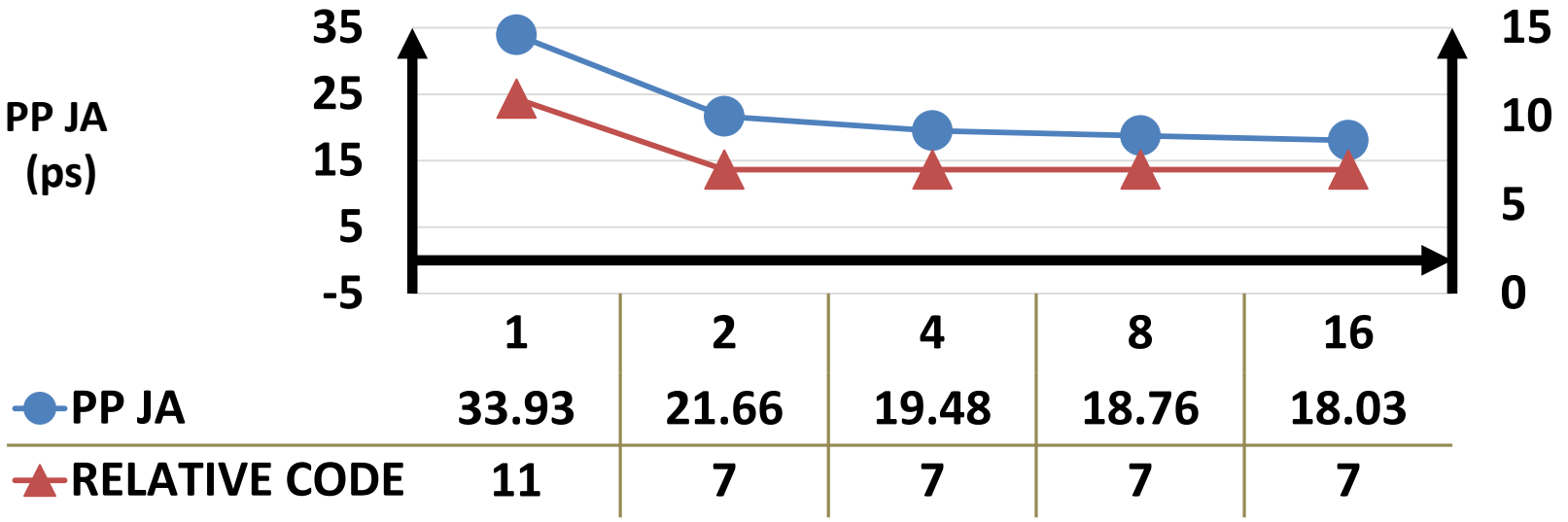


[11] E. Gantsog, D. Liu, A. B. Apsel, "0.89 mW on-chip jitter-measurement circuit for high speed clock with sub-picosecond resolution", *Proc. IEEE Eur. Solid-State Circuits Conf.*, pp. 457-460, Sep. 2016.

[14] P.-Y. Chao, C.-W. Tzeng, S.-Y. Huang, C.-C. Weng, S.-C. Fang, "Process Resilient Low-Jitter All-Digital PLL via Smooth Code Jumping", *IEEE Trans. on VLSI Systems*, vol. 21, no. 12, pp. 2240-2249, Dec. 2013.

The relative peak-to-peak Jitter amount code from jitter measurement and peak-to-peak Jitter of clock under measurement from ADPLL versus the different initial suppression threshold of suppression filter in ADPLL

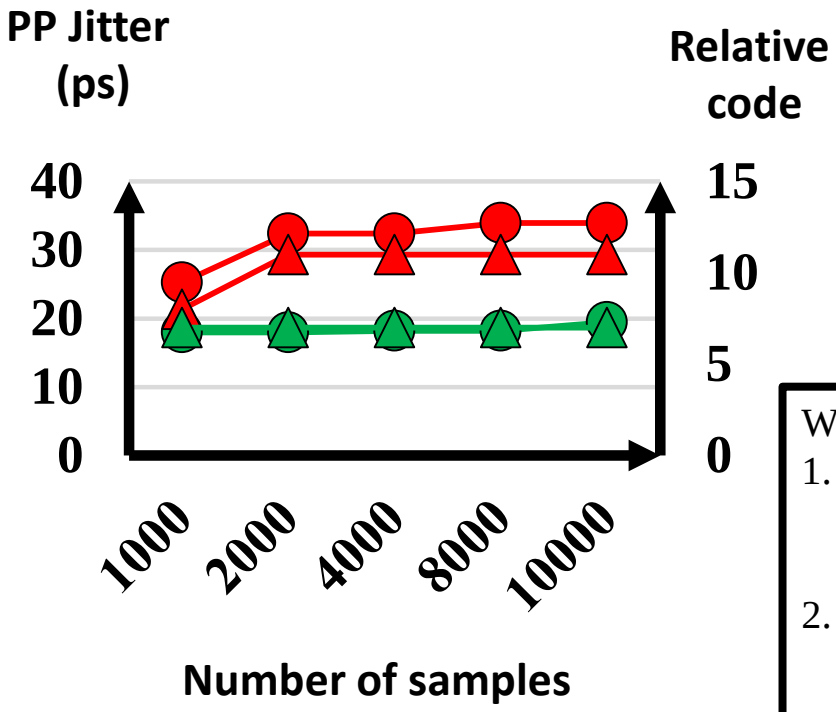
The number of samples for different Initial suppression threshold is 10000.



The relative peak-to-peak Jitter amount code from jitter measurement and peak-to-peak Jitter of clock under measurement from ADPLL versus the different number of samples (Table)

Number of samples		1000	2000	4000	8000	10000
Initial Suppression Threshold = 1	PP Jitter (ps)	25.24	32.39	32.39	33.93	33.93
	Code	8	11	11	11	11
Initial Suppression Threshold = 4	PP Jitter (ps)	17.95	17.95	18.20	18.20	19.48
	Code	7	7	7	7	7

The relative peak-to-peak Jitter amount code from jitter measurement and peak-to-peak Jitter of clock under measurement from ADPLL versus the different number of samples (Table)



- CODE for the initial suppression threshold is 1.
- PP Jitter for the initial suppression threshold is 1.
- CODE for the initial suppression threshold is 4.
- PP Jitter for the initial suppression threshold is 4.

We can get **the following information** from this figure:

1. The peak to peak jitter from the output clock of ADPLL is **highly positive correlated** to the relative code of jitter measurement.
2. The peak to peak jitter from the output clock of ADPLL will **eventually reach saturation with increasing the number of period samples in the measurement interval.**

Comparison with other works

	[2](2005)	[5](2009)	[8](2011)	[9](2011)	[12](2019)	This Work
Technology	0.18um	90nm	90nm	65nm	28nm	90nm
Data processing method	Off Chip	Off Chip	Off Chip	Off Chip	Off Chip	On Chip
Input frequency	100MHz	2.5GHz	3GHz	100MHz ~ 300MHz	1.06GHz	1GHz
Area (mm^2)	0.004	0.075	0.038	0.0027	0.0029	0.014
Power (mw)	N/A	N/A	11.4 @3GHz	0.6 @100MHz	1.1	3.0 @1GHz
RMS-jitter (ps) (oscilloscope/BIJM) or PK-PK jitter (ps) (waveform parser /BIJM)	RMS: 42.70/62.70	RMS: 10.10/6.20	RMS: 4.15/3.78	RMS: 1.90/1.99	PK-PK: 15.60/10.80	
Error	46.8%	39.0%	8.9%	4%	44.4%	
Experimental results	Measured					Simulated

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Conclusion

- The proposed solution is **fully cell based design** by using 90nm cell library (easy process migration)
- Our proposed solution can **record all incoming period samples in real time** so that we can report the relative code implies the peak-to-peak jitter among all incoming period samples.
- According to transistor-level simulation result, our proposed solution demonstrates the **highly positive correlation between its input (i.e., the p-p jitter of clock under measurement.) and its output (i.e., digital code.)** for convincing users the credibility of our proposed solution.
- **The area of proposed jitter measurement is 63.6% of that of ADPLL.**
  - 0.014 mm^2.
- The **power** of proposed jitter measurement is about **3.01mW**.
- **The margin of checking window is sufficient** for ensuring the function of min max TDC(i.e., measure the period samples in real time.) and **it is scalable** for different application.

Thanks for your attention!

References

[1] K.A. Jenkins, A.P. Jose and D.F. Heidel, "An on-chip jitter measurement circuit with sub-picosecond resolution", *Proc. Of European Solid-State Circuits Conference (ESSCIRC)*, Vol. 22, No. 3, pp. 157-160, Sept. 2005.

[2] T. Xia, H. Zheng, J. Li and A. Ginawi, "Self-refereed on-chip jitter measurement circuit using Vernier oscillators", *Proc. of IEEE Computer Society Annual Symposium on VLSI*, May 2005.

[3] C.-Y. Li, C.-Y. Chou, and T.-Y. Chang. "A Self-Referred Clock Jitter Measurement Circuit in Wide Frequency Range."In Proc. IEEE 15th Asian Test Symp., pp.313-317, Nov. 2006.

[4] W. Tang, J. H. Feng, and C. L. Lee, "A Jitter Measurement Circuit Based On Dual Resolution Vernier Oscillator," Proceedings of the IEEE 8th International Conference on Asic, vols 1 and 2, pp. 1213-1216, 2009.

[5] S.Y. Jiang, K.H. Cheng and P.Y. Jian, "A 2.5-GHz built-in jitter measurement system in a serial-link transceiver," *IEEE Tran. Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 12, pp. 1698-1708, Dec. 2009.

[6] J. Yu and F. F. Dai, "On-chip jitter measurement using vernier ring time-to-digital converter," Asian Test Symposium, pp. 167-170, 2010.

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