A Delay-Adjustable, Self-Testable Flip-Flop for Soft-Error Tolerability and Delay-Fault Testability

Dave Y.-W. Lin, ChungLi Tang, and Charles H.-P. Wen
ECE Dept., NCTU, Taiwan

Outline

- Introduction
  - Enhancing Testability for Soft-Error Tolerance by DAST-FF
- Preliminary
  - DAD-FF: Soft-Error Tolerable Flip-Flop
- Method
- Experimental Results
- Conclusion

Introduction

Introduction (1/3)

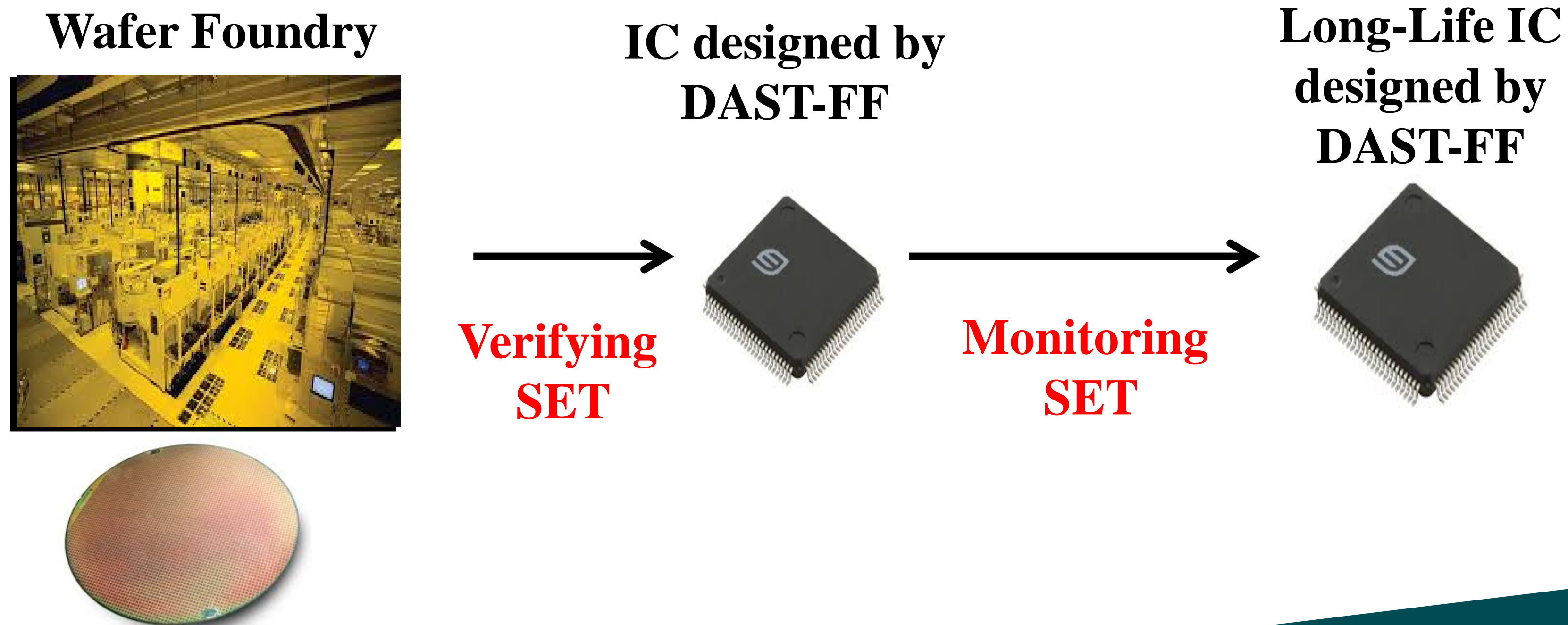
- In the general soft-error tolerable circuit design, its capability of soft-error tolerability (SET) is untestable and unverifiable, resulting in an unreliable system.
- From the perspective of design for testability (DUT), the untestable SET is not acceptable.

Introduction (2/3)

- As a result, we extend our previous radiation-hardened design: Delay-Adjustable D-Flip-Flop (DAD-FF) as Delay-Adjustable and Self-Testable Flip-Flop (DAST-FF).
- Both DAD-FF and DAST-FF are hardened by delay latching (detailed in Preliminary).

Introduction (3/3)

- To sum up, our proposed DAST-FF can (1) verify SET after manufactured, and (2) monitor SET during IC's life time.



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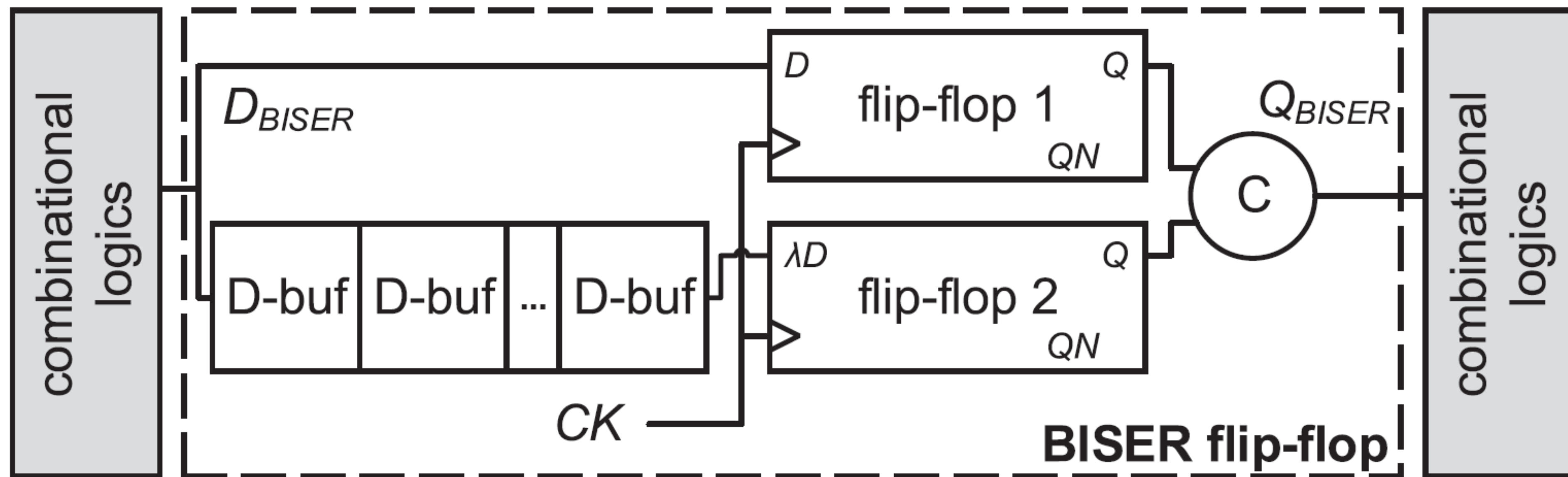
2. Preliminary

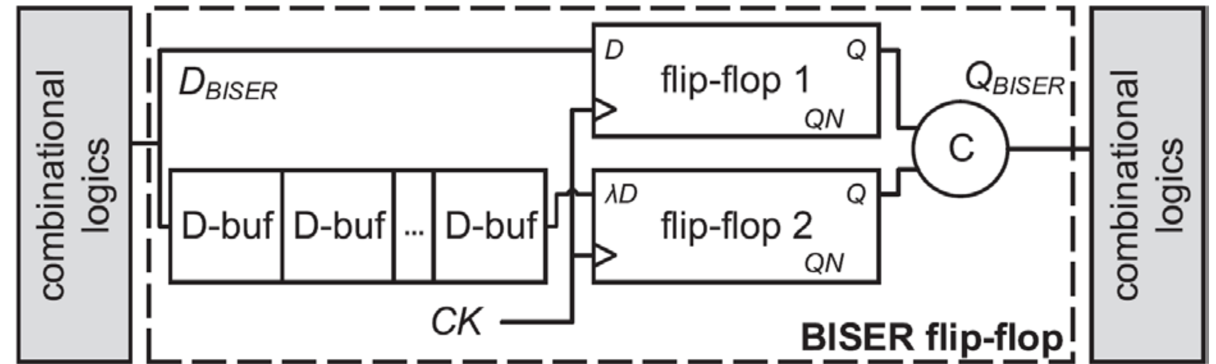
Delay-Latching Technique (1/3)

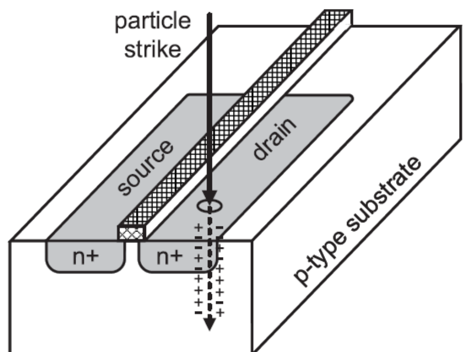
- The basis of DAST-FF: DAD-FF and BISER, which utilize the latching delay for detecting soft errors.

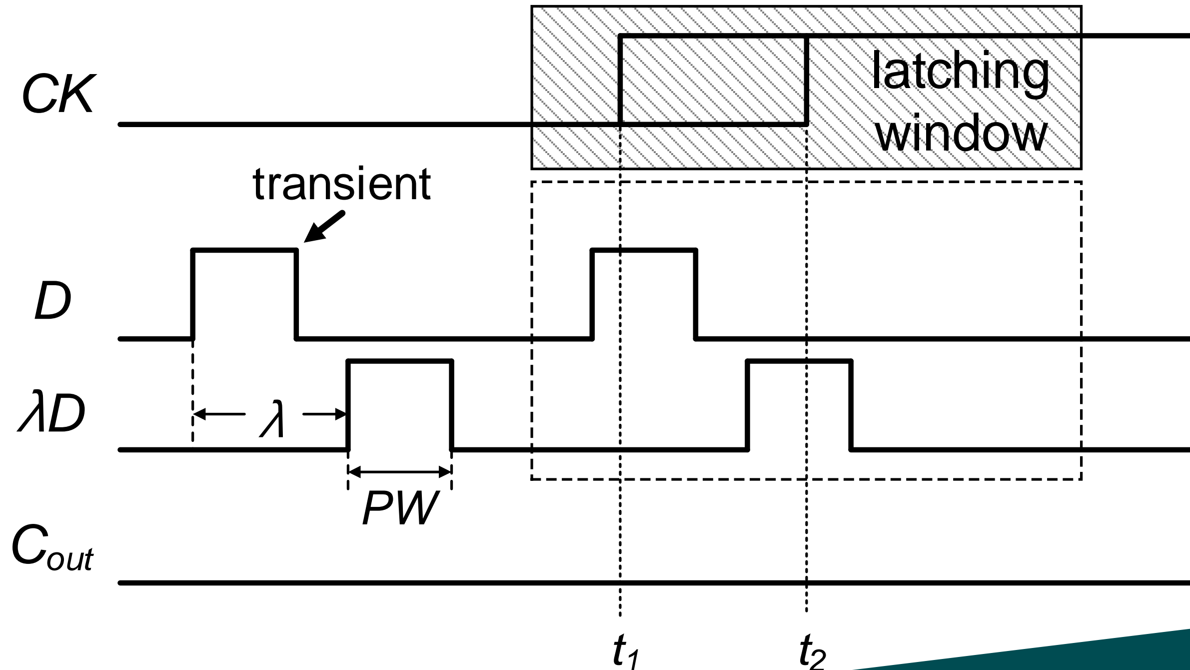


Delay-Latching Technique (2/3)

- Dual-module redundancy
  - Typical data path
  - Delayed data path







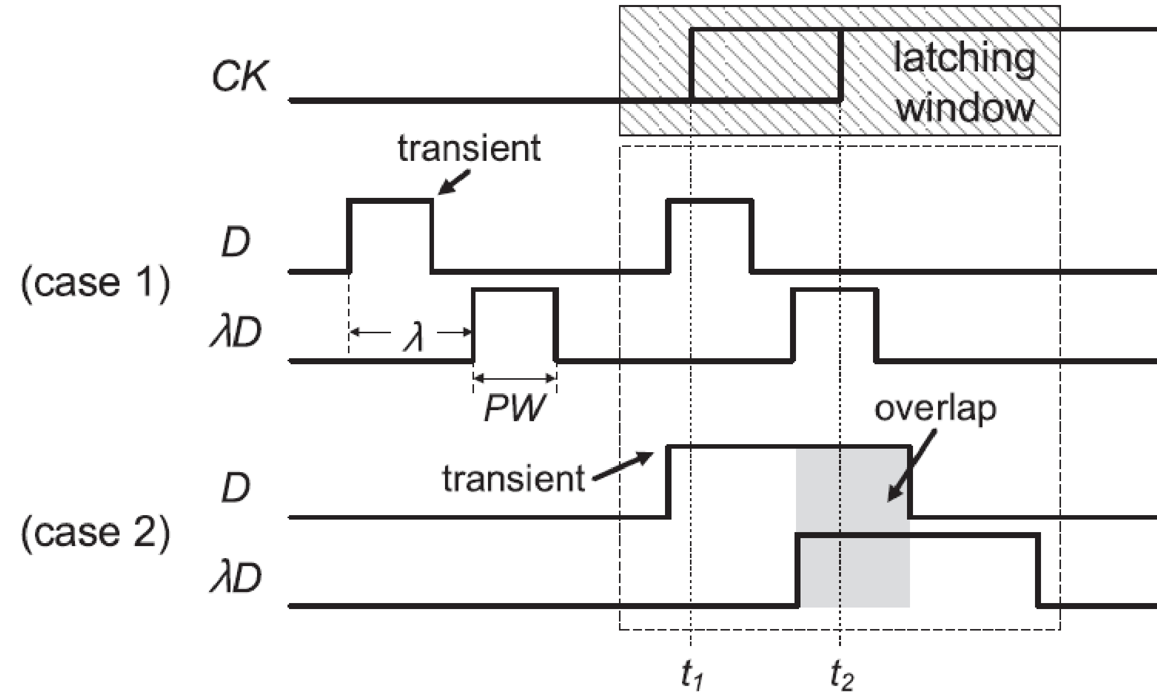
D	λD	Z
0	0	0
1	1	1
1	0	RT
0	1	RT

Truth table of C-element

Delay-Latching Technique (3/3)

Case 1: latching delay λ > PW

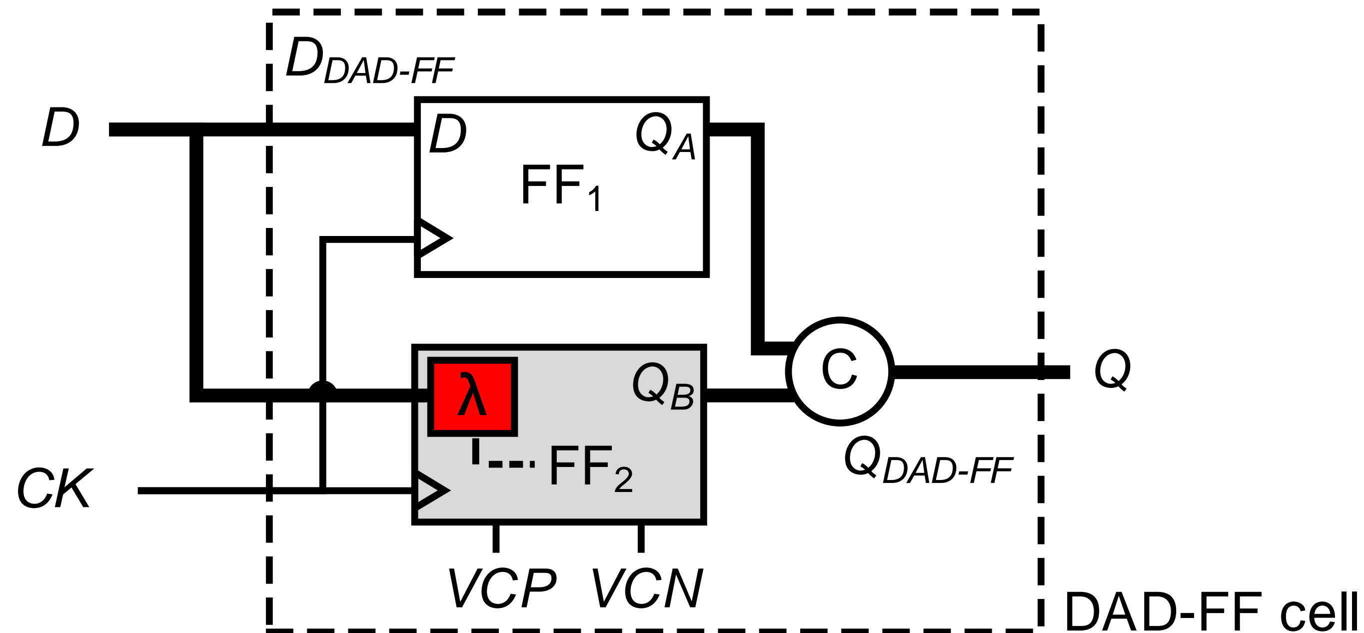
Case 2: latching delay λ < PW



- Transient in gray area are undetectable, indicating that λ has significant impact on SET.

Recap DAD-FF and λ

- Dual data path (original and delayed data path)
- λ is the key factor to detect soft errors.

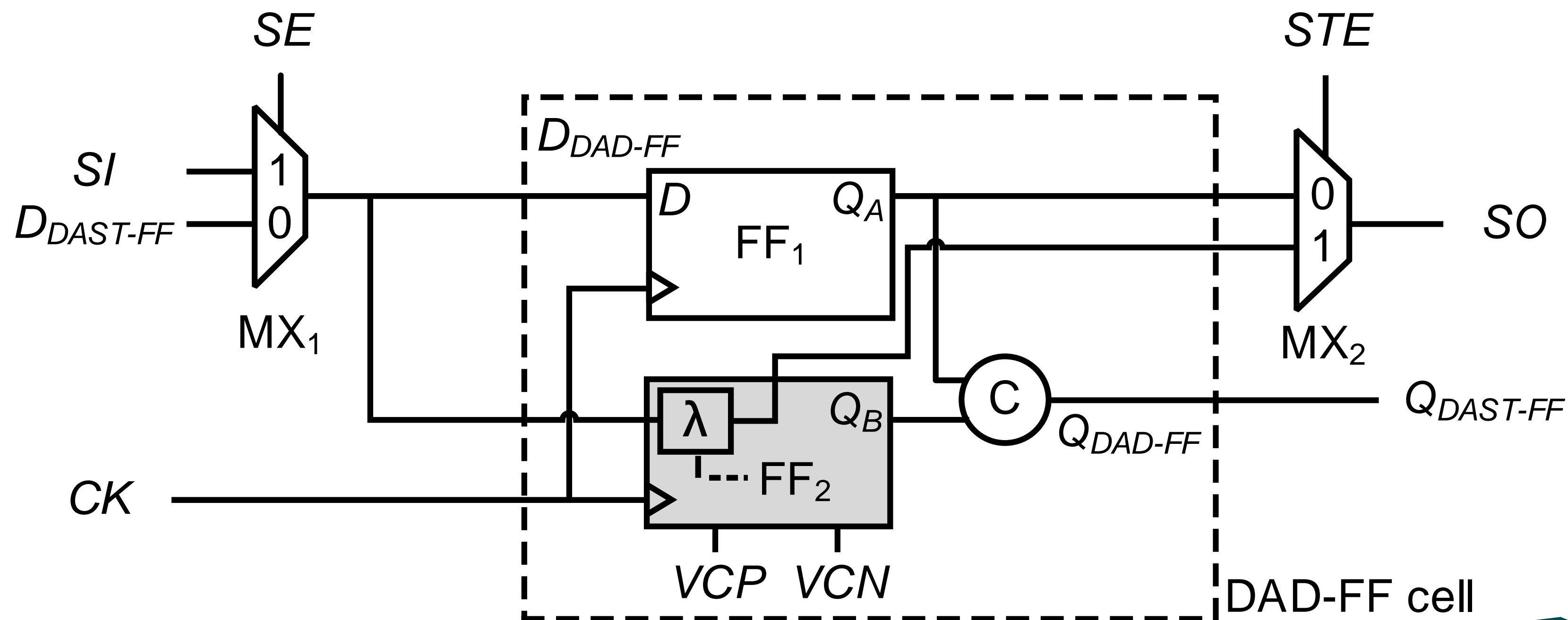


3.

DAST-FF: Delay-Adjustable and Self-Testable Flip-Flop

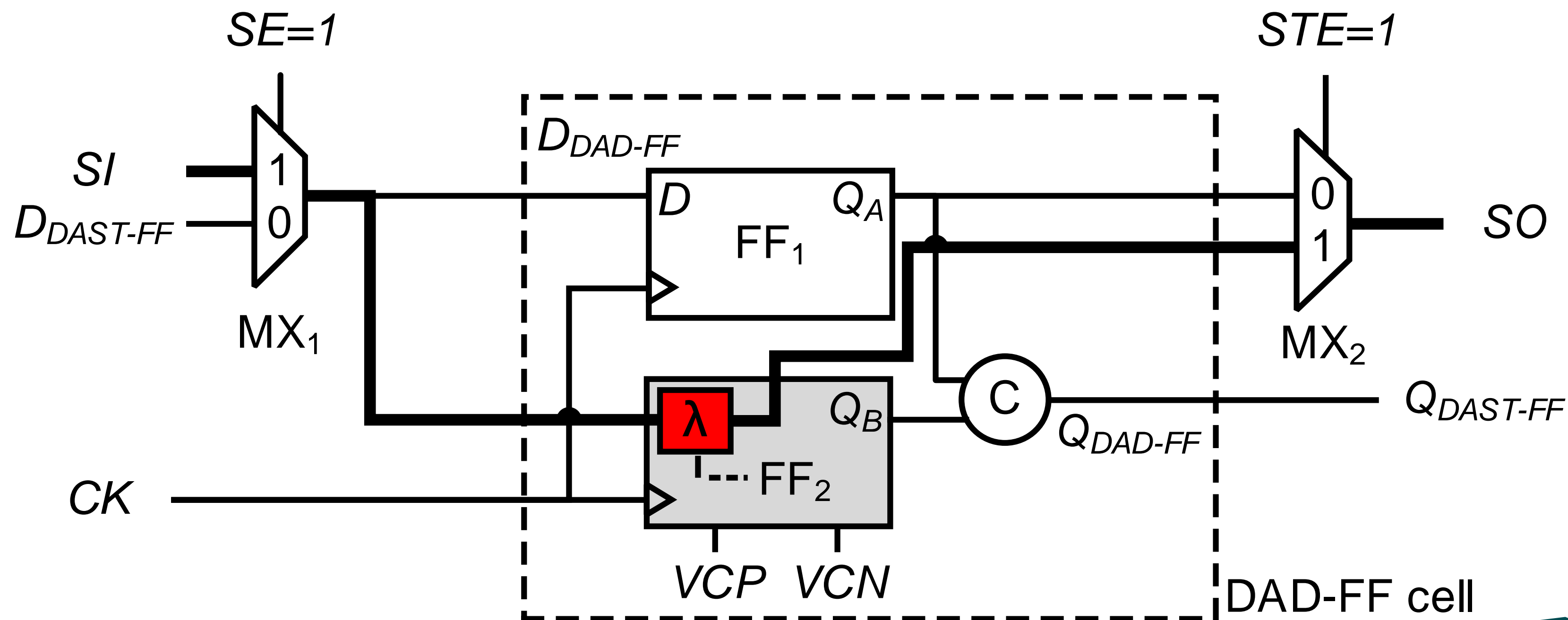
DAST-FF (1/2)

- The major purpose of DAST-FF is to make λ testable.
- The second purpose of DAST-FF is scannable.



DAST-FF (2/2)

- SE (scan enable) = 1, STE (self-test enable) = 1
- In NanGate45, $Delay_{SI-SO} = 278$ps ($\lambda = 166$ps)



$\lambda = 166$ps can achieve >6 σ protection (99.99983% particles)

Built-In Self-Test for λ

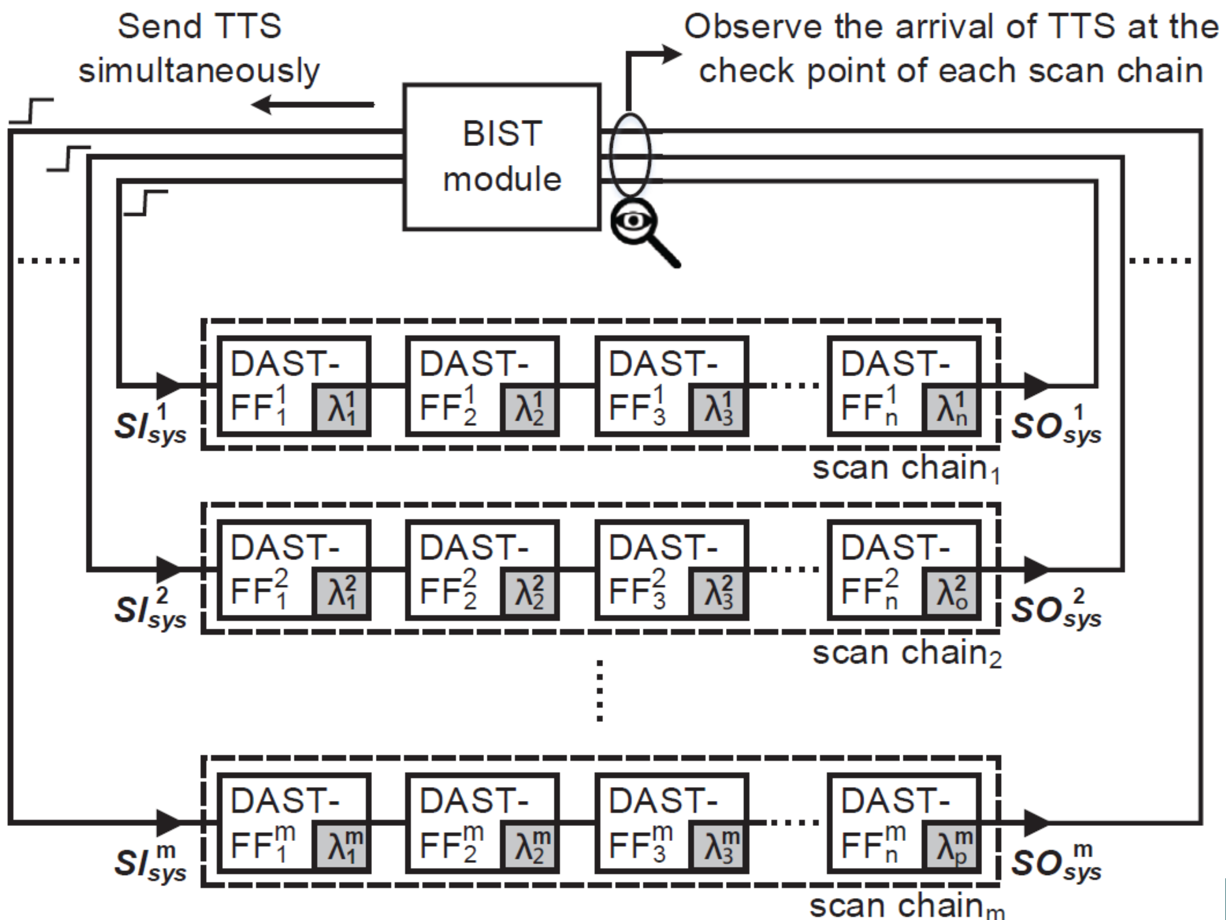
- Accumulating λs for better testability
  - Single λ is too tiny
  - Increase the overall BIST time

SE=1
STE=1
SI
$D_{DAST\text{-}FF}$
1
0
MX_1
$D_{DAD\text{-}FF}$
D
Q_A
FF_1
0
1
SO
MX_2
λ
Q_B
FF_2
C
$Q_{DAST\text{-}FF}$
CK
VCP VCN
DAD-FF cell

SI_{sys}
DAST-FF_1 λ_1
DAST-FF_2 λ_2
DAST-FF_3 λ_3
DAST-FF_n λ_n
SO_{sys}
t=0
t=0 $t=\lambda_1+\epsilon_1$
t=0 $t=\lambda_1+\epsilon_1+\lambda_2+\epsilon_2$
t=0 $t=\sum_{i=1}^{n}(\lambda_i+\epsilon_i)$

Concurrent BIST for λ

For multiple scan-chain design

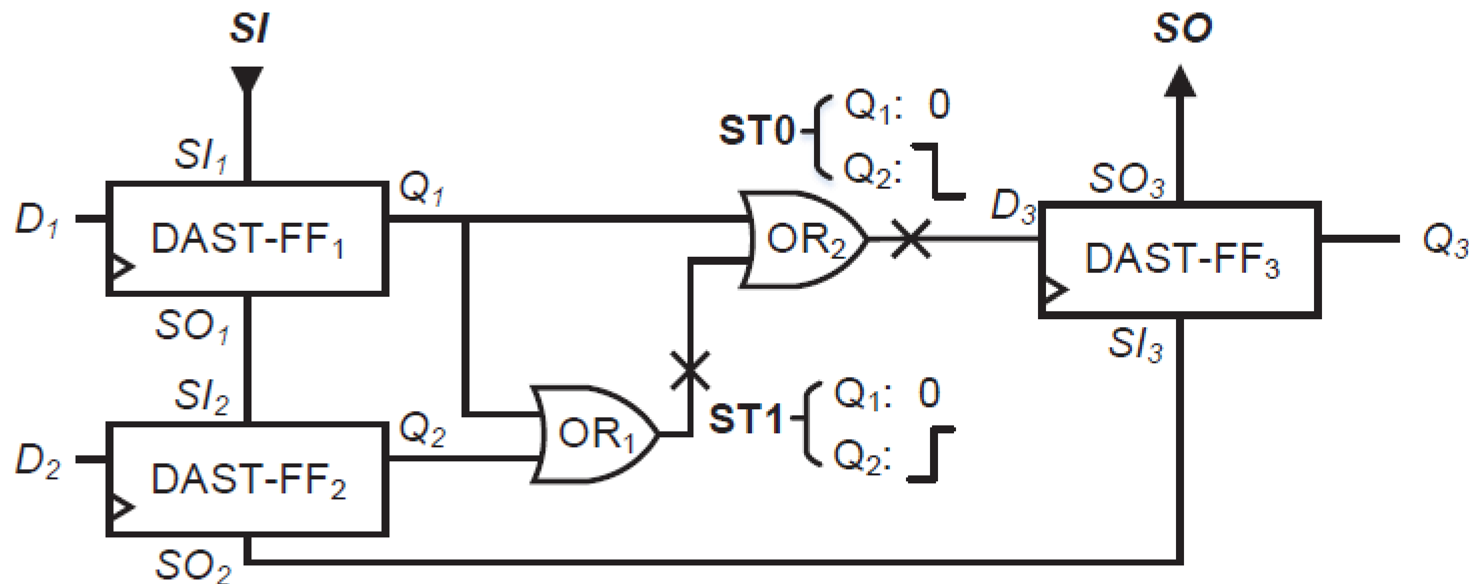


Advantage:

- Concurrent λ self test
- Minimize test time
- No additional routing or placing requirement

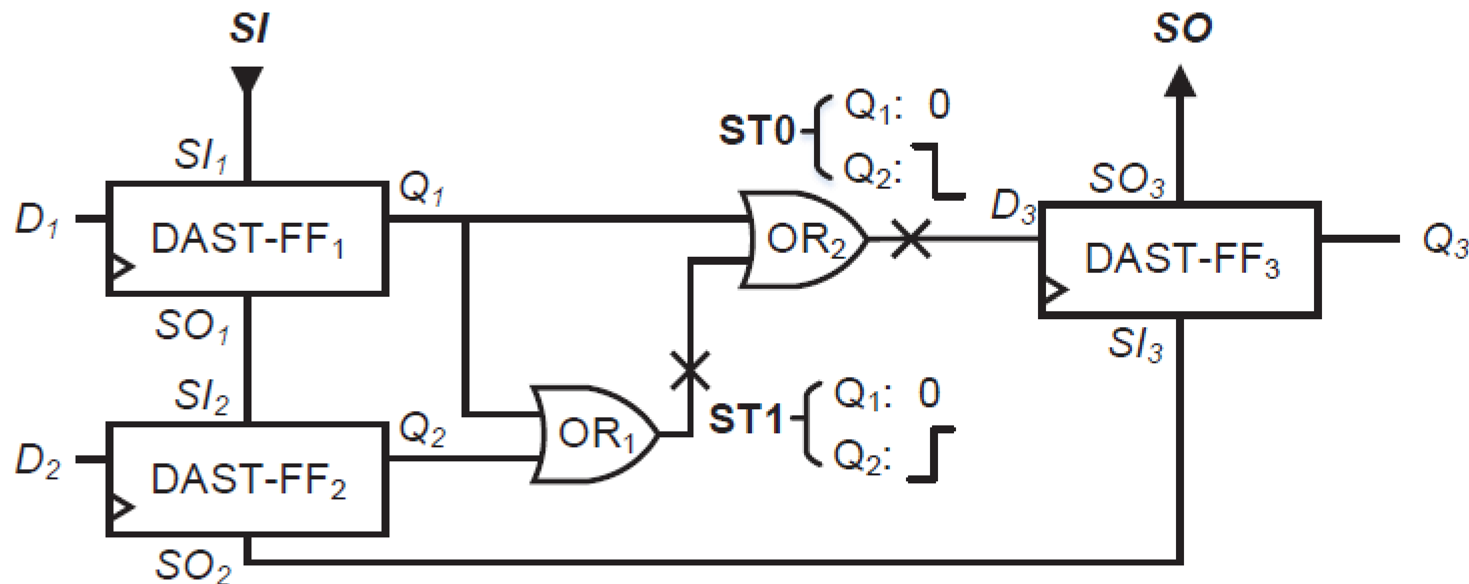
Delay-Fault Testing (1/2)

- DAST-FF increases testability on delay faults
  - ST0: slow-to-0 fault
  - ST1: slow-to-1 fault



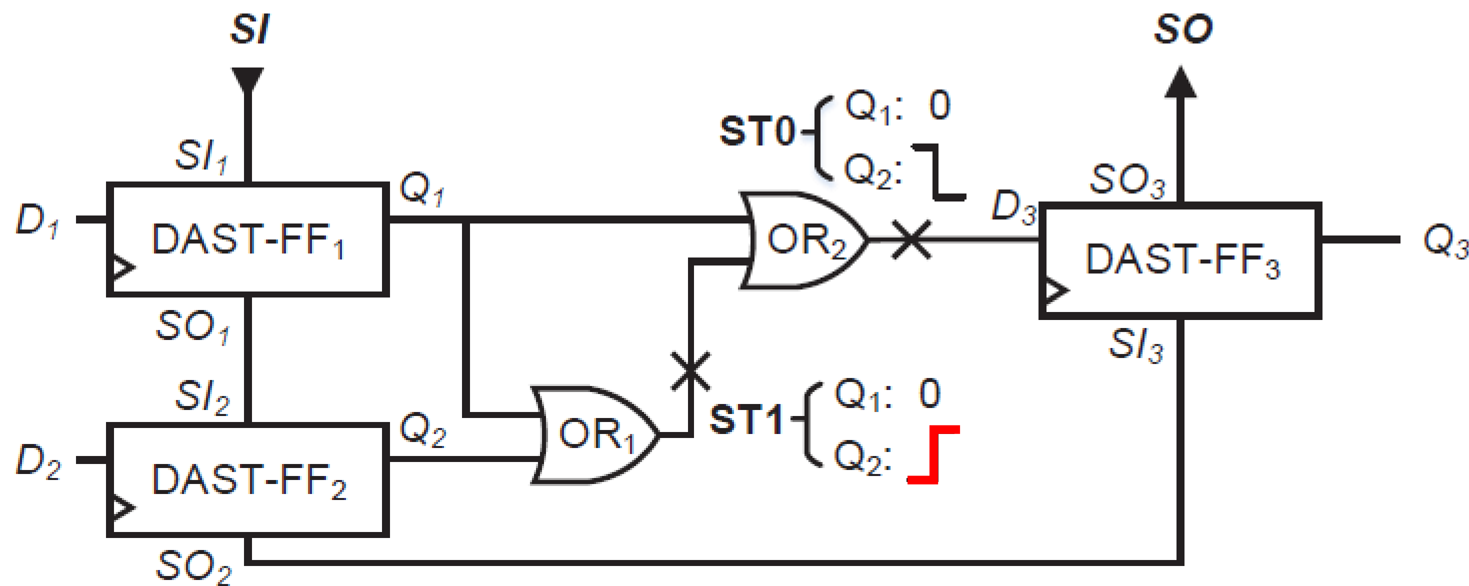
Delay-Fault Testing (2/2)

- Traditional Launch on Capture (LOC) and Launch on Shift (LOS) cannot detect such ST1.



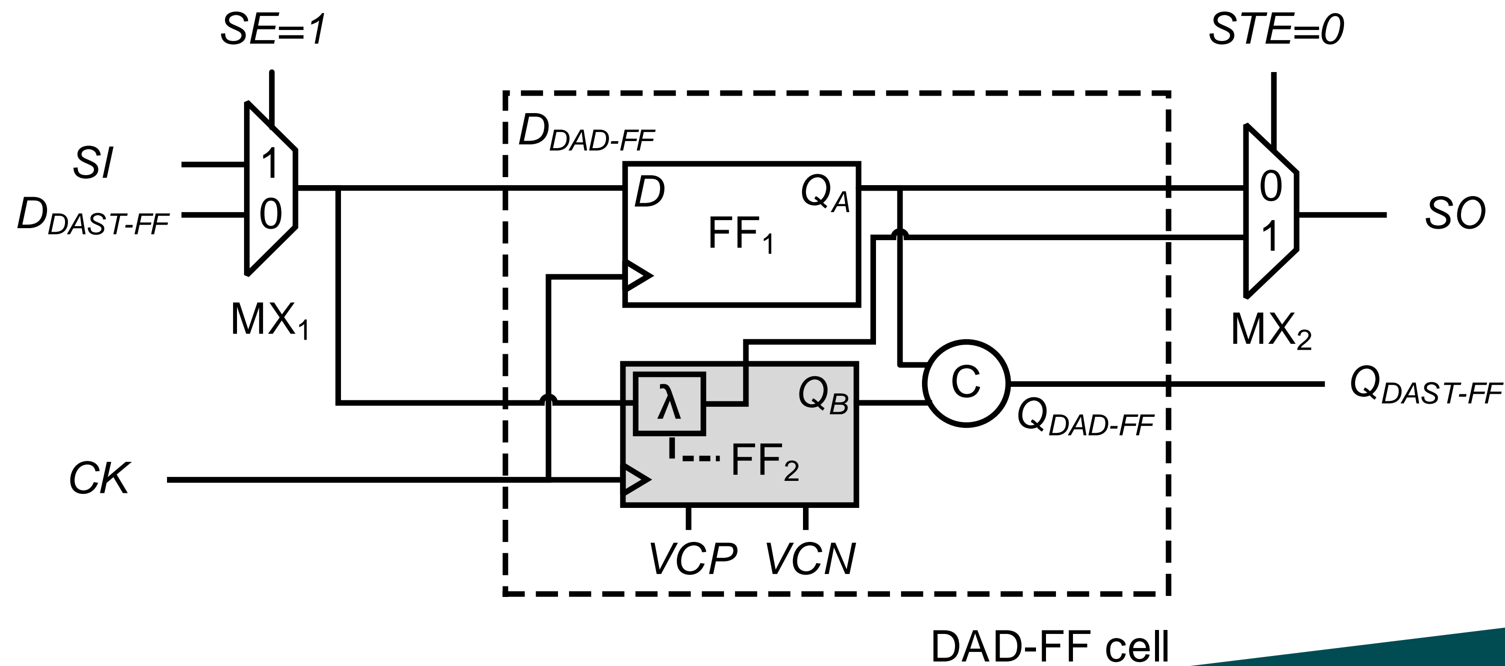
Enhanced Delay-Fault Testing (1/4)

- Enhanced scan-delay test:
  - Generate arbitrary transition in each FF
  - Method: add additional latch to store complementary values



Enhanced Delay-Fault Testing (2/4)

- Our DAST-FF has dual storage nodes originally.



Enhanced Delay-Fault Testing (3/4)

- Our DAST-FF has dual storage nodes originally.
- Transmission gate (TG) is added to store complementary values

Enhanced Delay-Fault Testing (4/4)

2. Turn off TG, retain TP_1 at Q

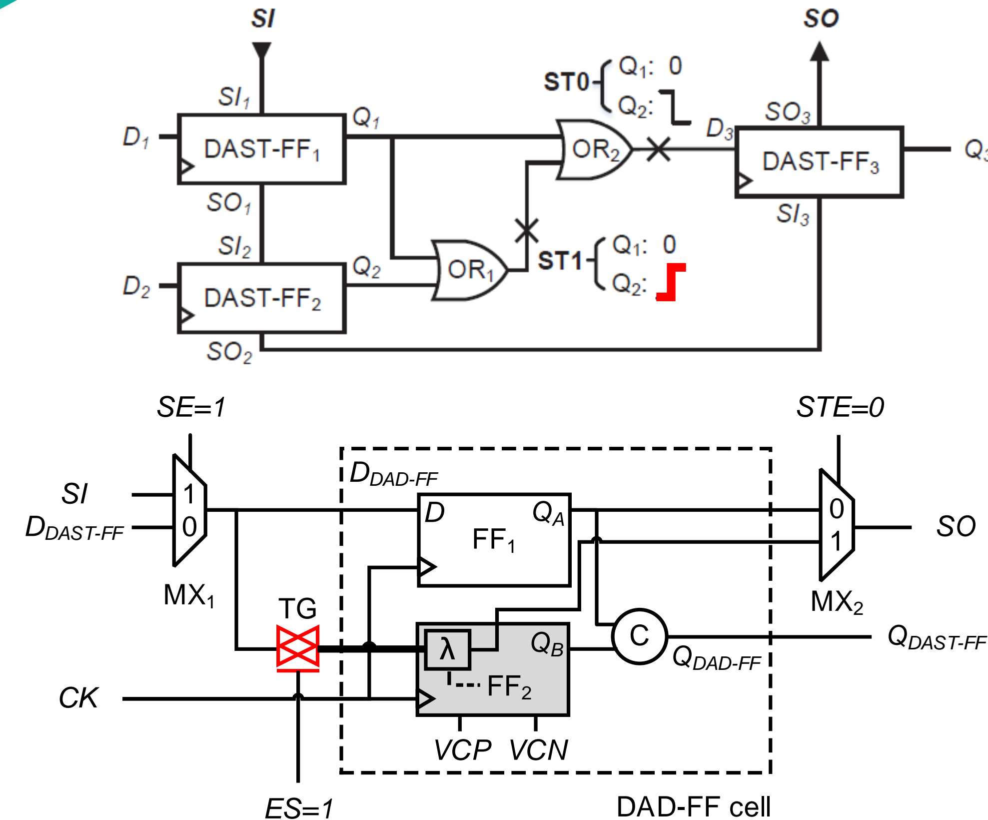
4. Turn on TG, generate transition at Q_2

cycle	1	2	3	4	5	6	7
	SI Q	SI Q	SI Q	SI Q	SI Q	SI Q	Q
$DAST\text{-}FF_1$	1 1	0 0	0 0	1 0	1 0	0 0	0
$DAST\text{-}FF_2$		1 1	0 0	0 0	1 0	**1 0**	
$DAST\text{-}FF_3$			1 1	0 1	0 1	1 1	

1. Scan in TP_1

3. Scan in TP_2

4. Activate ST1, and capture ST1 at D_3

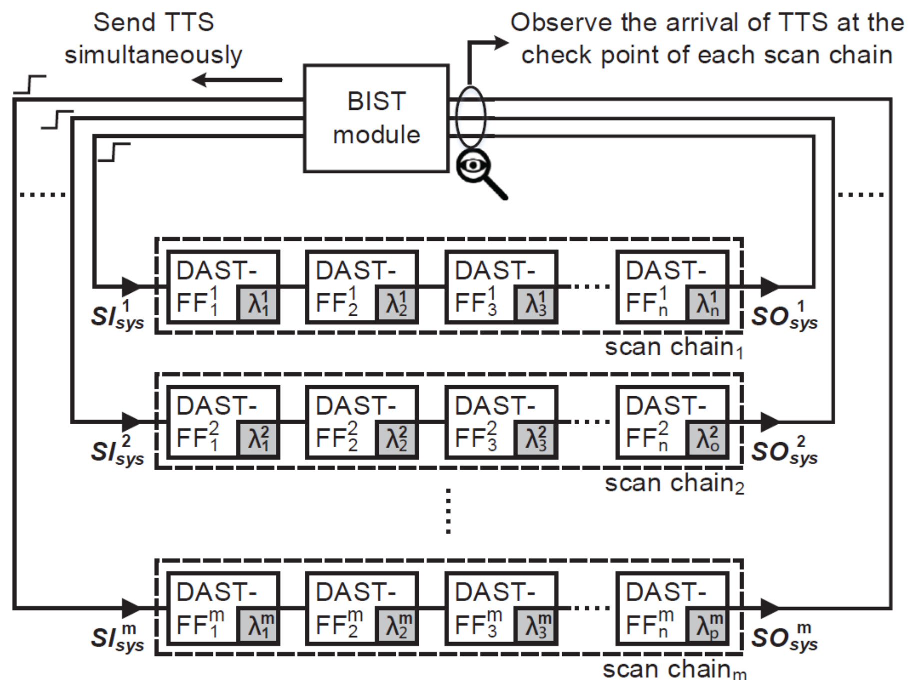


1. Scan in TP_1=001
2. Turn off TG and retain TP_1 at FF_1
3. Scan in TP_2=011
4. Turn on TG and generate a rising transition

Experimental Results

Experimental Results

- Experimental results can be divided into 2 parts:
  - λ-based BIST
  - Enhanced delay-fault testing



2. Turn off TG, retain TP_1 at Q

4. Turn on TG, generate transition at Q_2

cycle	1	2	3	4	5	6	7
	SI Q	SI Q	SI Q	SI Q	SI Q	SI Q	Q
$DAST\text{-}FF_1$	1 1	0 0	0 0	1 0	1 0	0 0	0
$DAST\text{-}FF_2$		1 1	0 0	0 0	1 0	**1 0**	
$DAST\text{-}FF_3$			1 1	0 1	0 1	1 1	

1. Scan in TP_1

3. Scan in TP_2

4. Activate ST1, and capture ST1 at D_3

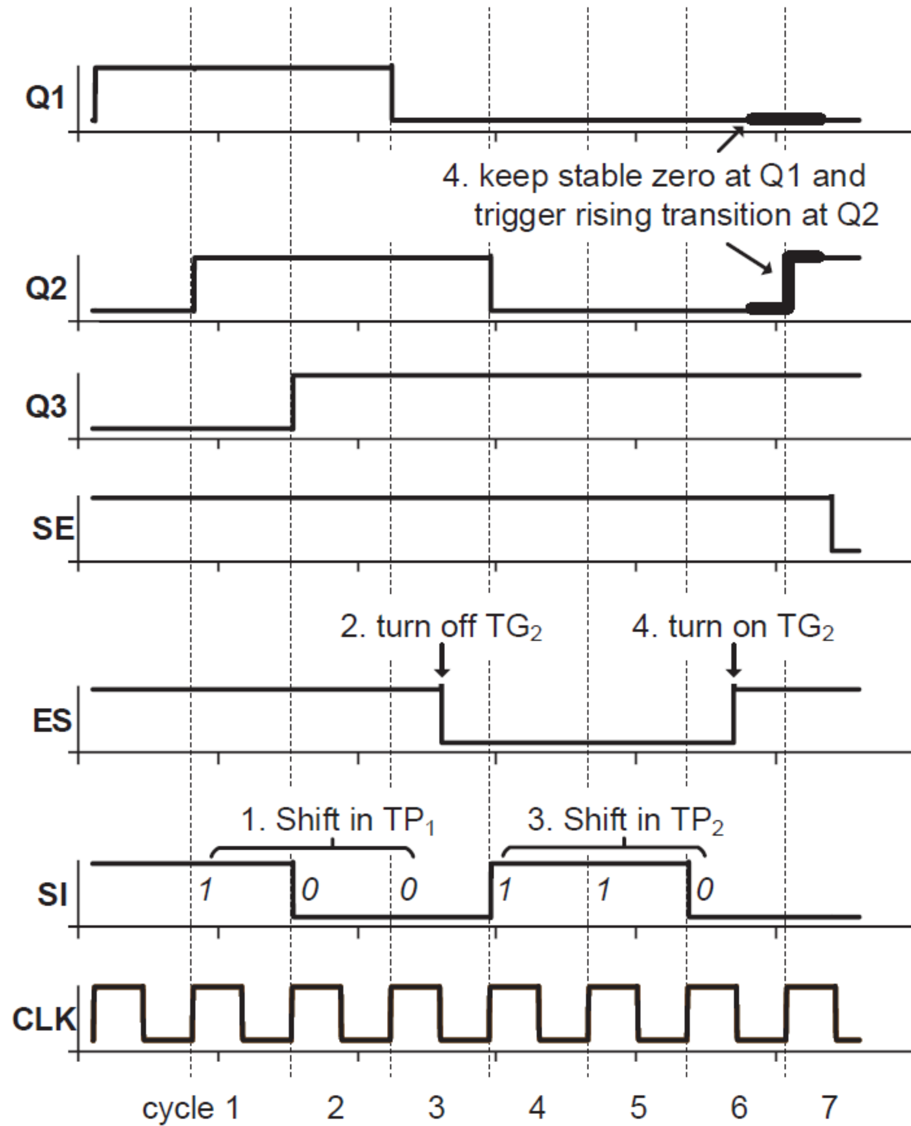
λ-Based Concurrent BIST

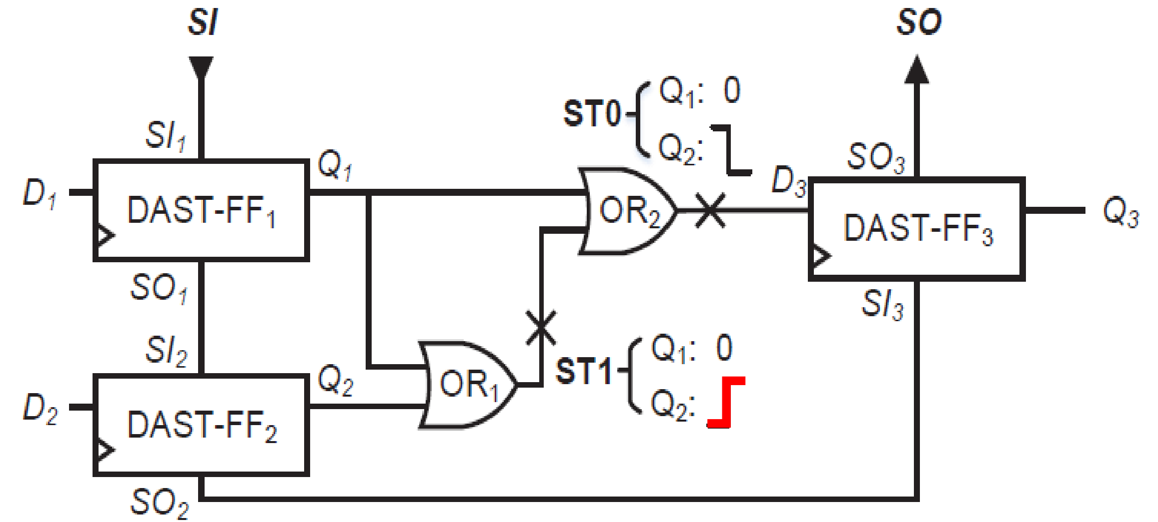
TABLE I
UTILIZING SELF-TEST MODE TO ESTIMATE ACCUMULATED DELAYS OF THE SCAN CHAIN BY DAST-FF FOR SOFT-ERROR-TOLERABILITY VERIFICATION

	DMA by DAST-FF		des_perf by DAST-FF					
# of DAST-FF/ total gates	2192/ 25301		8802/ 111229					
# of scan chain	SC = 1		SC = 3					
# of DAST-FF in scan chain	N = 2192		N_1 = 3405		N_2 = 3217		N_3 = 2180	
Intrinsic delay ϵ (ns)	0.112		0.112		0.112		0.112	
latching delay λ (ns)	0.145	0.166	0.145	0.166	0.145	0.166	0.145	0.166
Target energy level LET (MeV-cm^2/mg)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)	20 ($> 3\sigma$)	32 ($> 6\sigma$)
Overall delay (Λ) of scan chain $\Lambda = N \times (\lambda + \epsilon)$ (ns)	563.3	609.4	875.1	946.6	826.8	894.3	560.3	606.0
Check point (CP) in BIST $CP = \Lambda / T_{clk}$ (cycle)	563	609	875	946	826	894	560	606

*Given the clock period in the BIST circuit is $T_{clk} = 1$ ns.

Enhanced Delay-Fault Testing





2. Turn off TG, retain TP_1 at Q

4. Turn on TG, generate transition at Q_2

cycle	1	2	3	4	5	6	7
	SI Q	SI Q	SI Q	SI Q	SI Q	SI Q	Q
$DAST\text{-}FF_1$	1 1	0 0	0 0	1 0	1 0	0 0	0
$DAST\text{-}FF_2$		1 1	0 0	0 0	1 0	**1 0**	
$DAST\text{-}FF_3$			1 1	0 1	0 1	1 1	

1. Scan in TP_1

3. Scan in TP_2

4. Activate ST1, and capture ST1 at D_3

Comparison

TABLE II
COMPARING PROPOSED DAST-FF WITH GENERIC DAD-FF, SCAN DAD-FF, SEU-TOLERANT ENHANCED SCAN FLIP-FLOP, AND GENERIC ENHANCED SCAN FLIP-FLOP

	Soft-error tolerability		Testability			Required resource	
	SET tolerable	SEU tolerable	Scannable	Enhance scan testable	Self testable	Number of additional controlling signals	Number of additional scan in/out
SFF [9]			✓			1 (SE)	2 (SI, SO)
DTES-FF [6]			✓	✓(stable)		2 (SE, HS)	2 (SI, SO)
ESFF-SED [10]		✓	✓	✓(stable)		2 (SE, HS)	2 (SI, SO)
UTES-FF [7]		✓	✓	✓(unstable)		2 (SE, CNF)	4 (SIP, SIN, SOP, SON)
DAST-FF	✓	✓	✓	✓**(stable)**	✓	**3 (SE, SD, ES)**	**2 (SI, SO)**

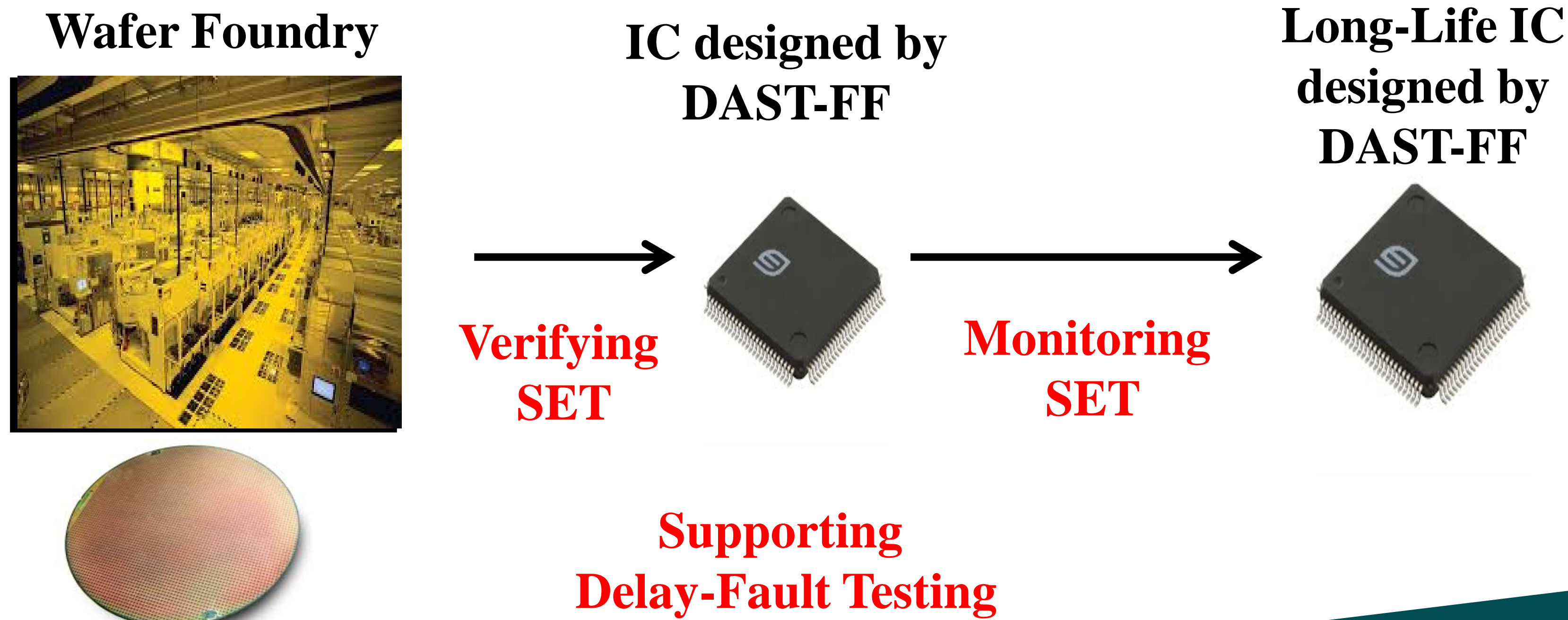
Conclusion

Conclusion (1/2)

- DAST-FF can not only tolerate soft-errors but also verify its soft-error tolerability by BIST.
- BIST module takes only 946ns for a design with 8802 FF to verify > 6σ soft-error protection.
- DAST-FF also supports enhanced delay-fault testing, incurring only 4.5% area overhead.

Conclusion (2/2)

- To sum up, our proposed DAST-FF can (1) verify SET after manufactured, and (2) monitor SET during IC's life time.



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